

FIG. 1C-1

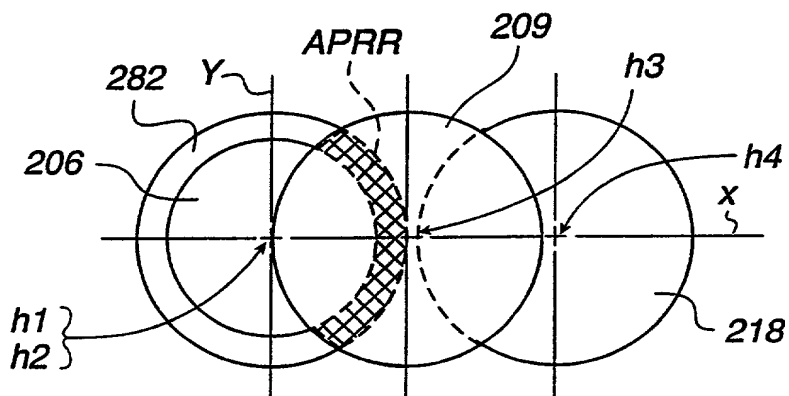


FIG. 1C-2

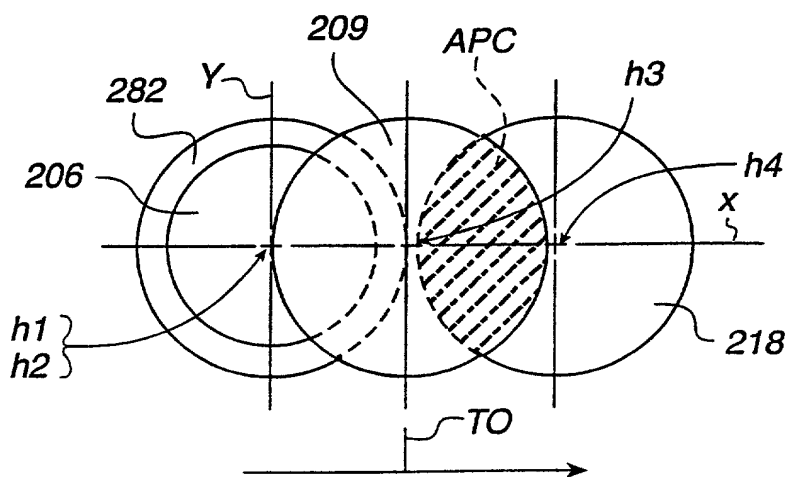


FIG. 1C-3

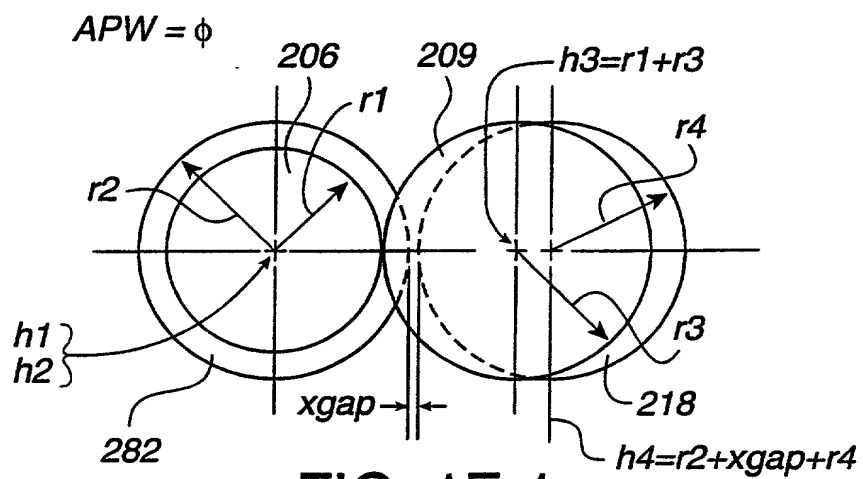


FIG. 1E-1

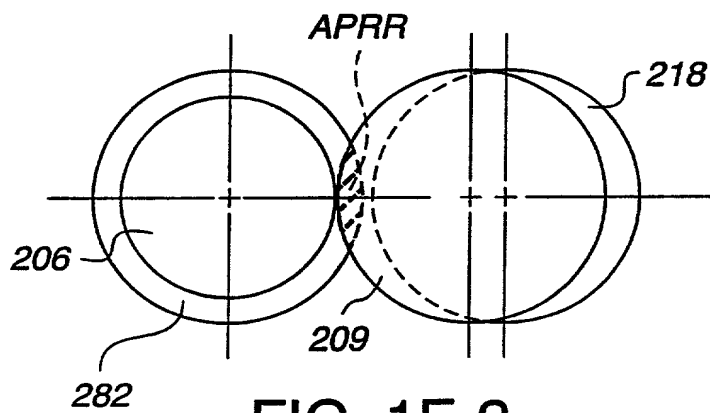


FIG. 1E-2

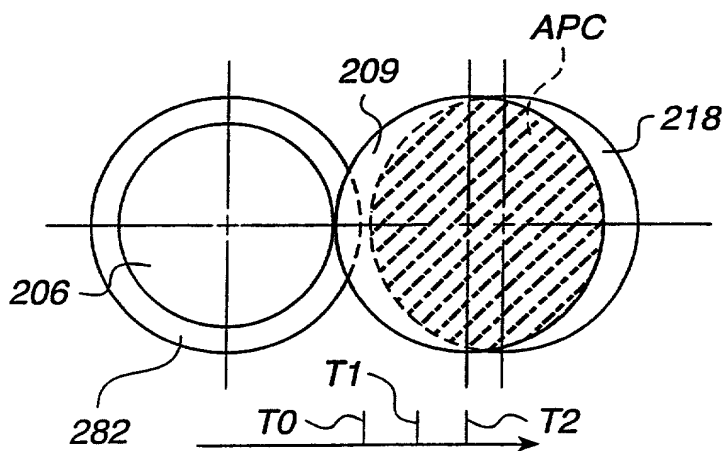


FIG. 1E-3

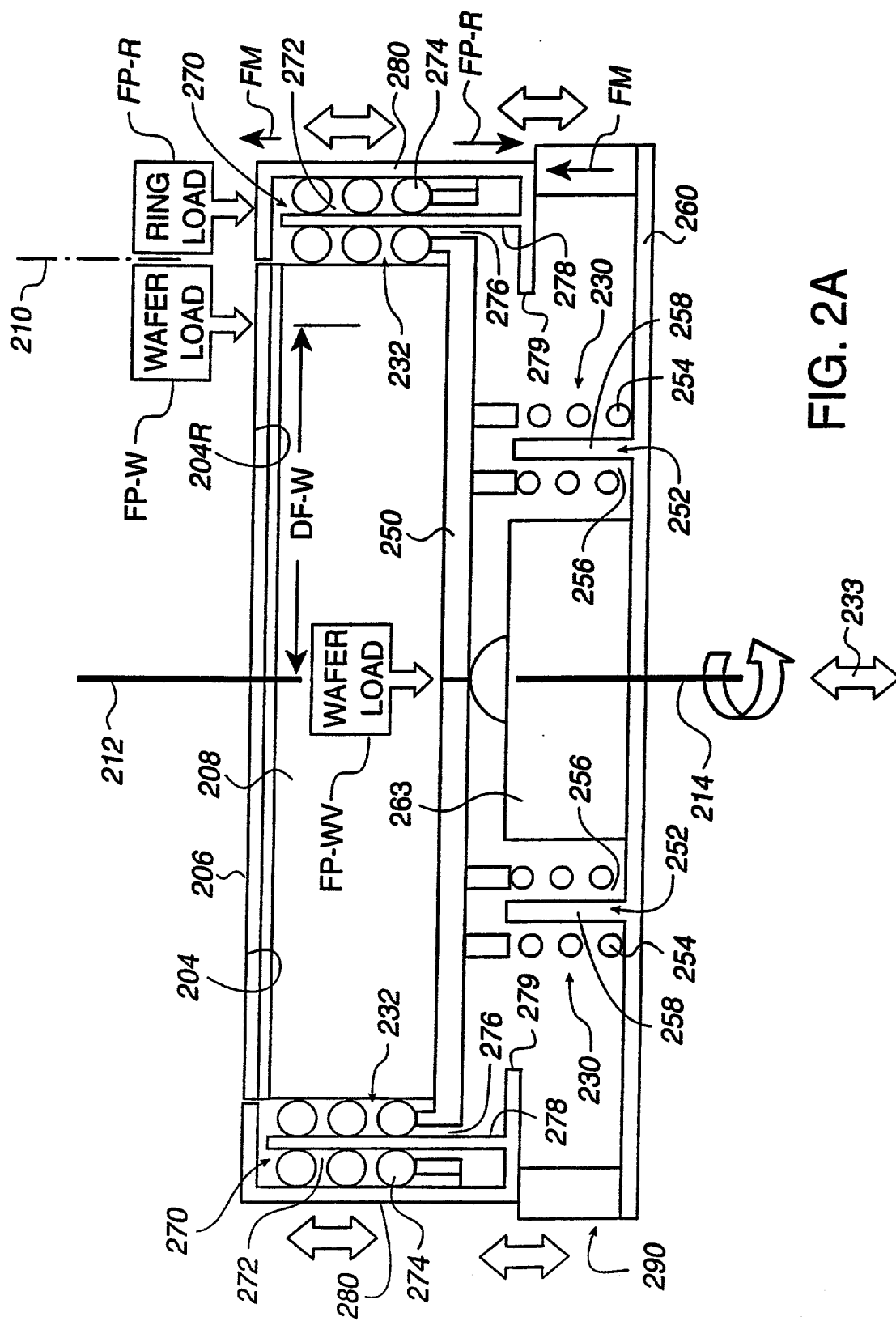
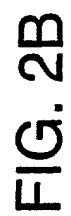


FIG. 2A



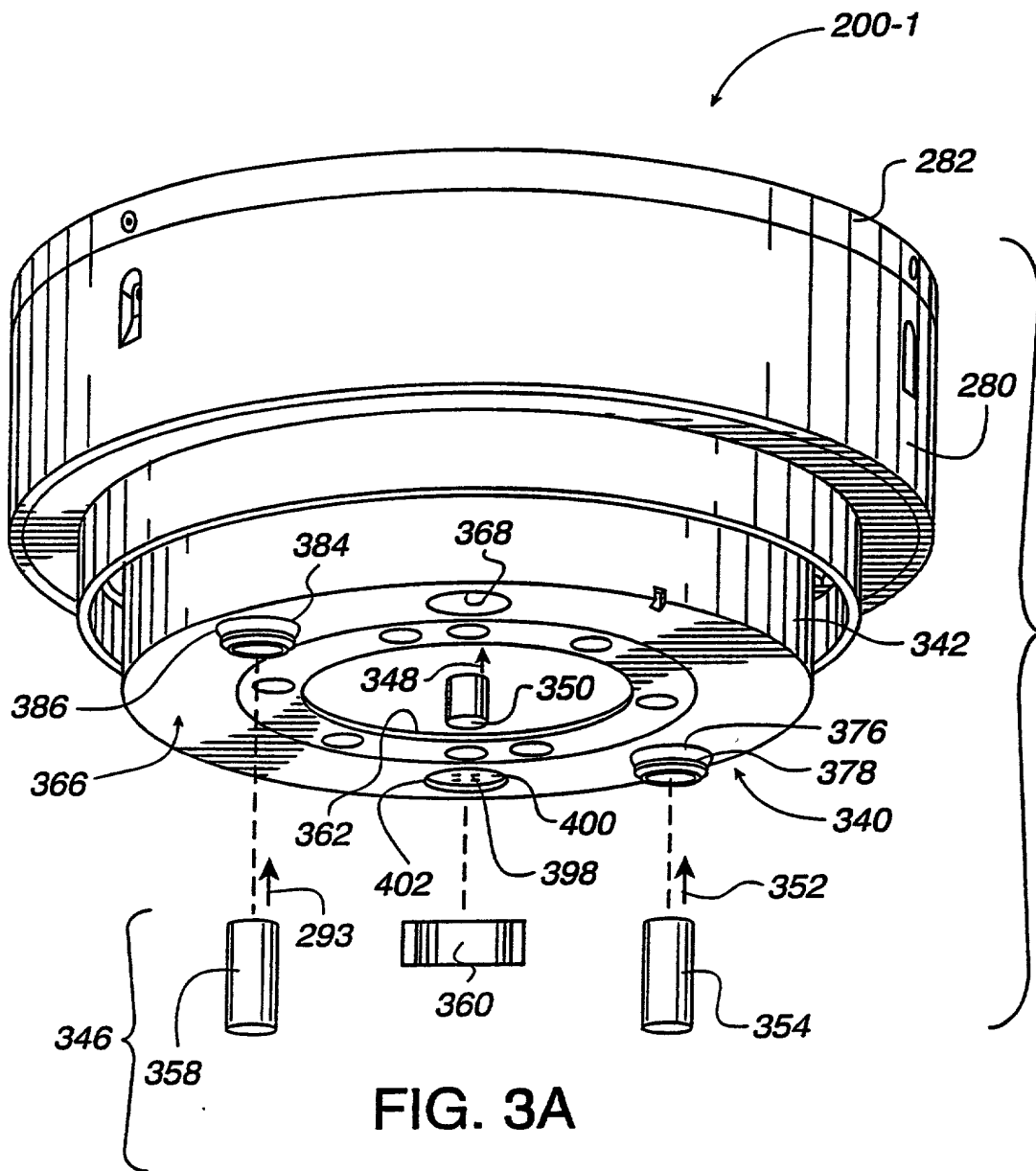


FIG. 3A

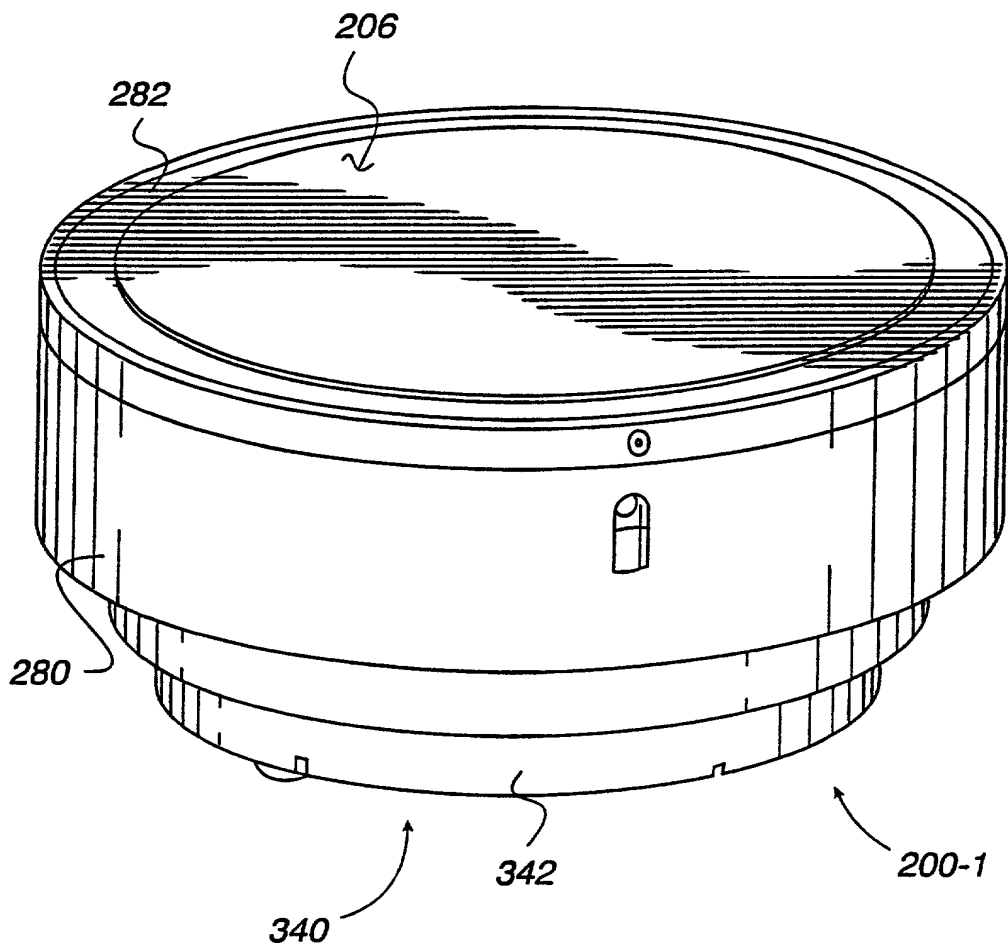


FIG. 3B

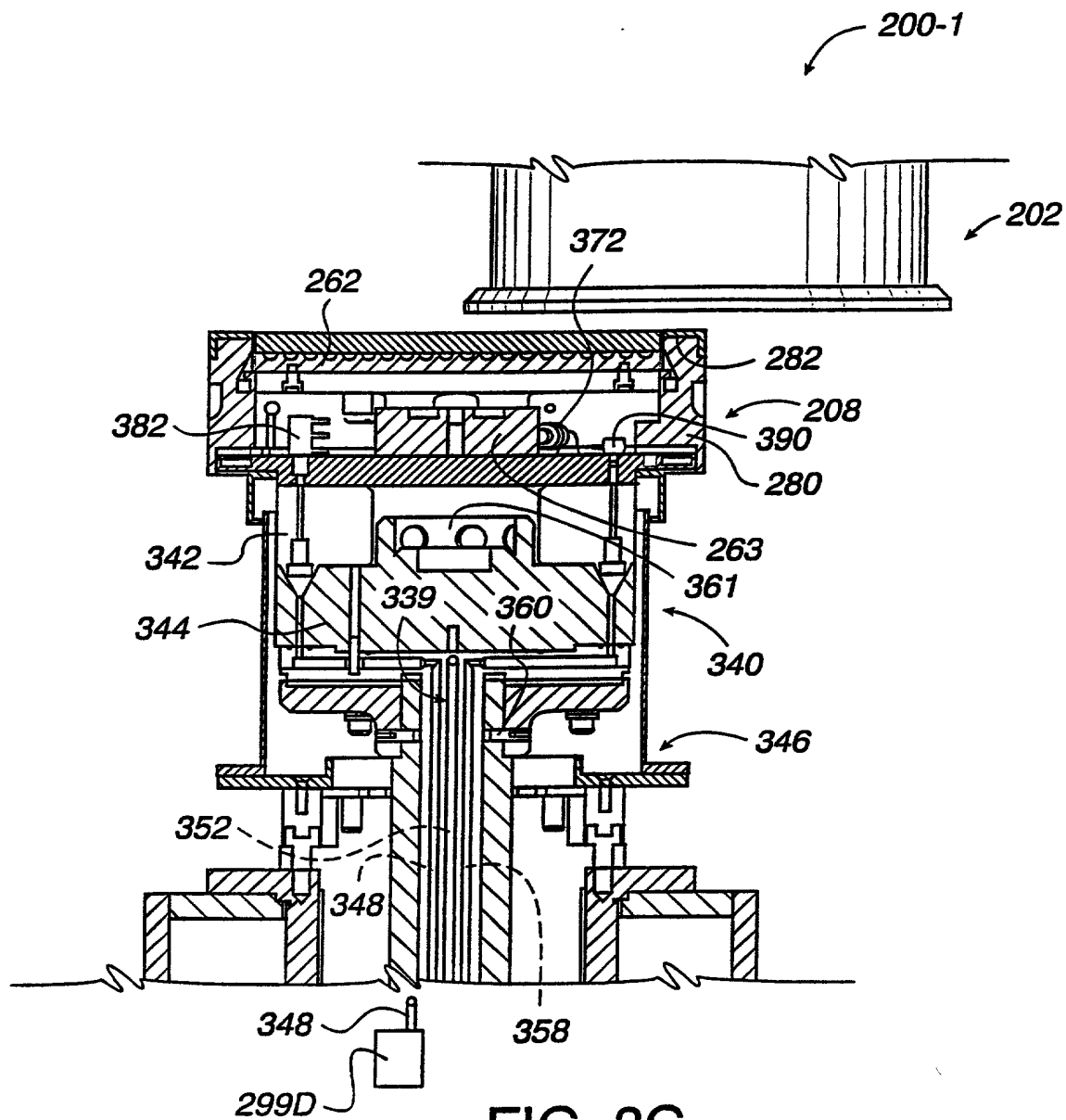


FIG. 3C

FIG. 4A

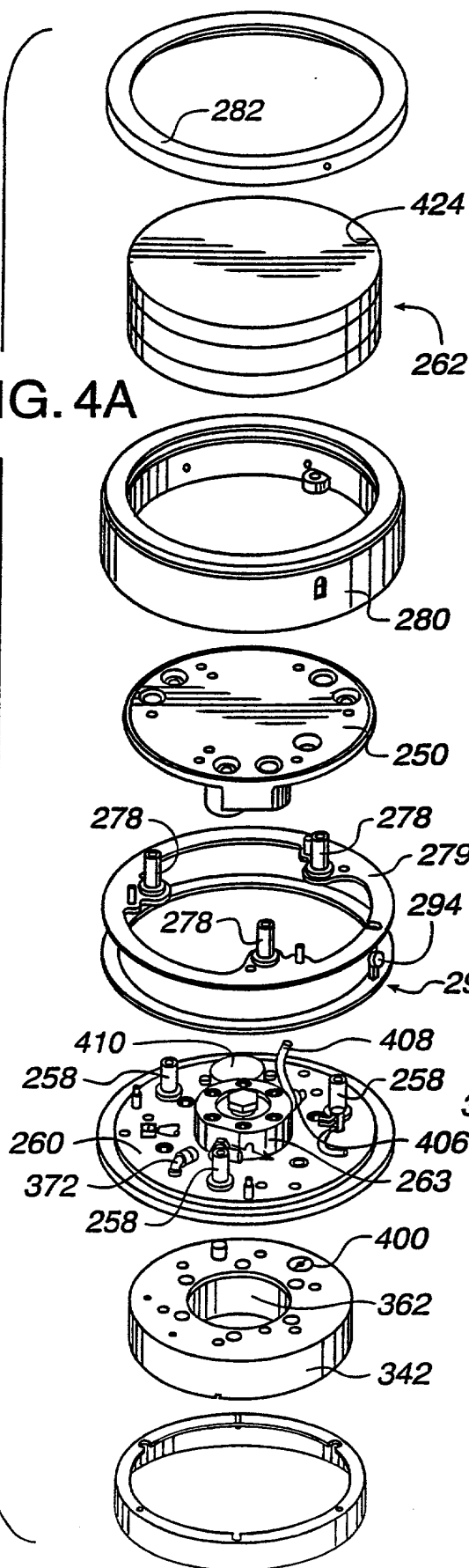
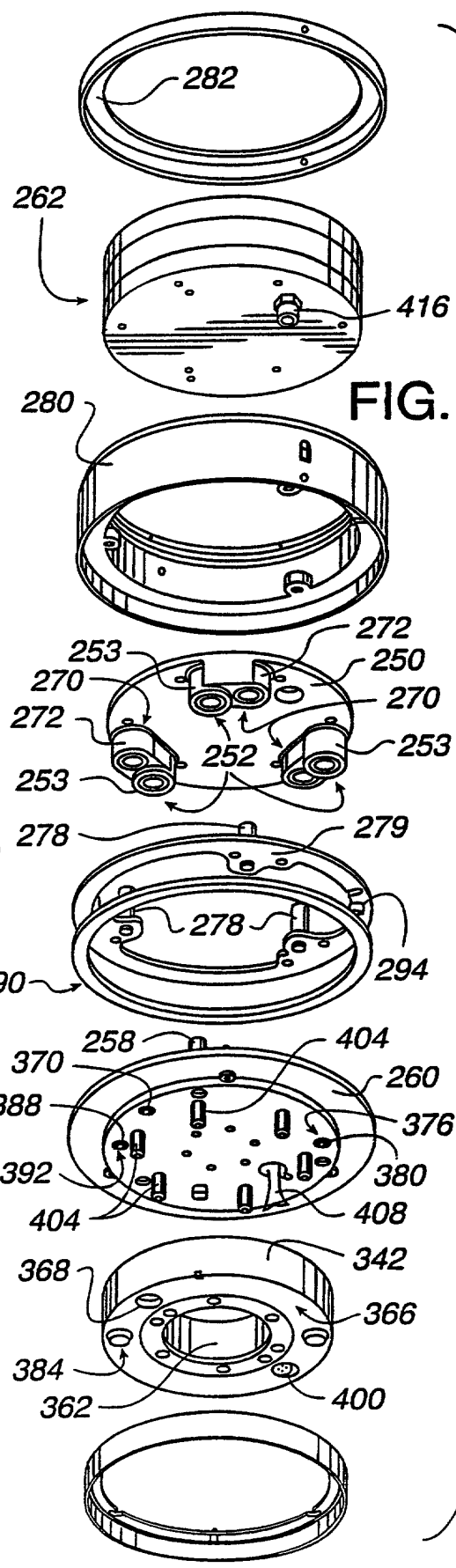
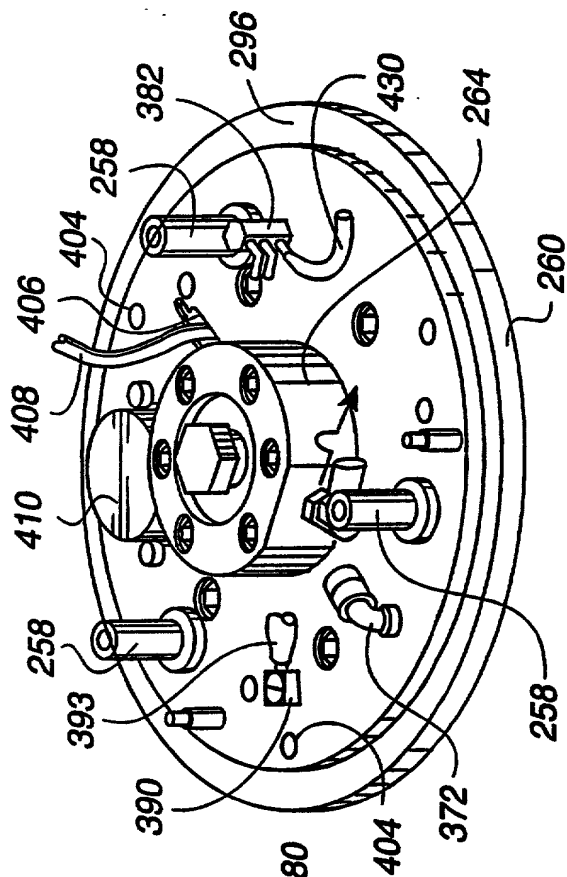
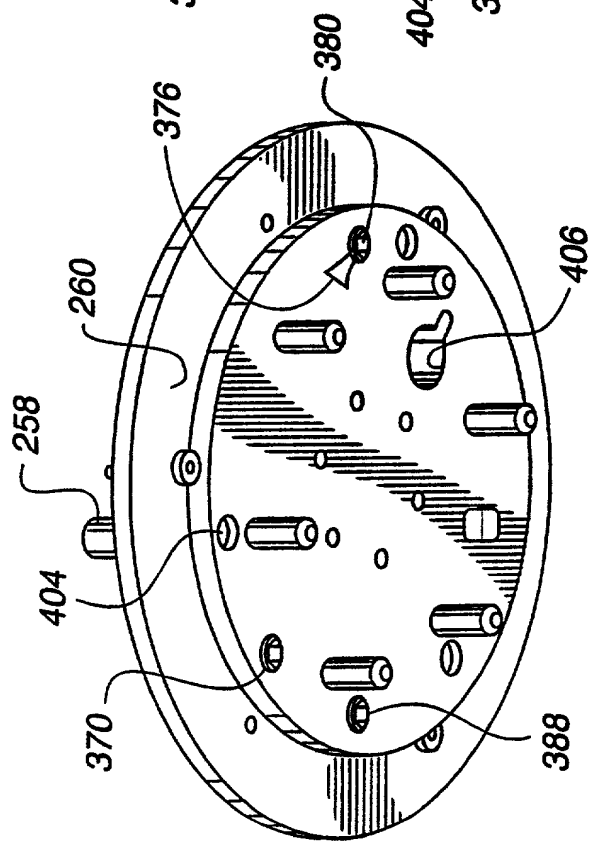


FIG. 4B





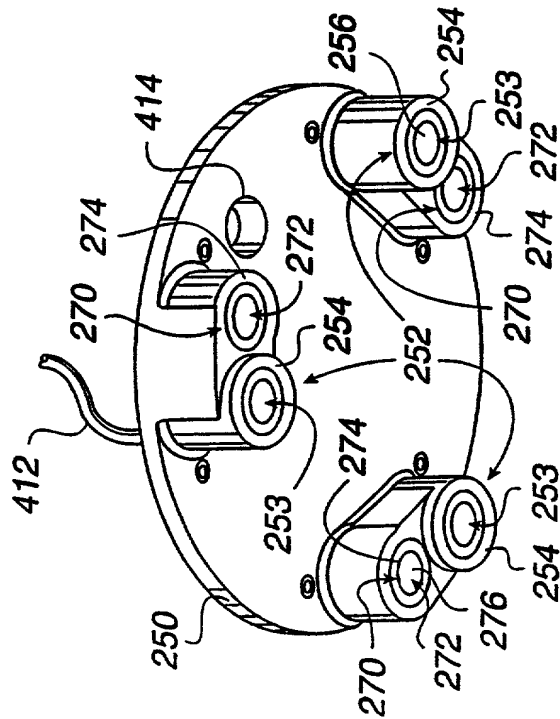


FIG. 5A-2

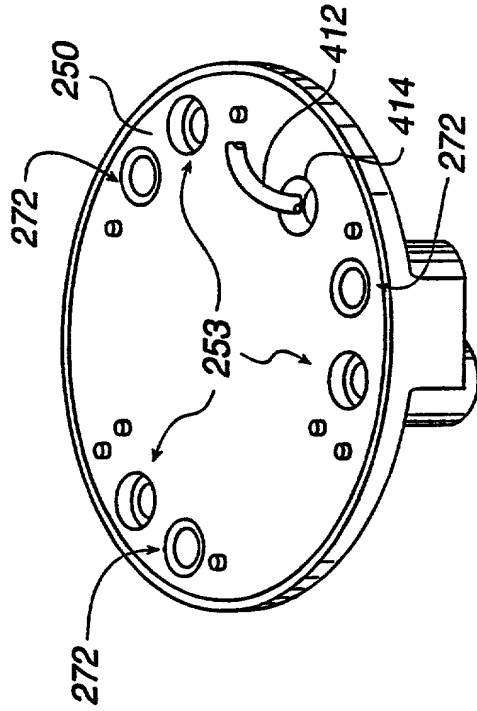


FIG. 5B-2

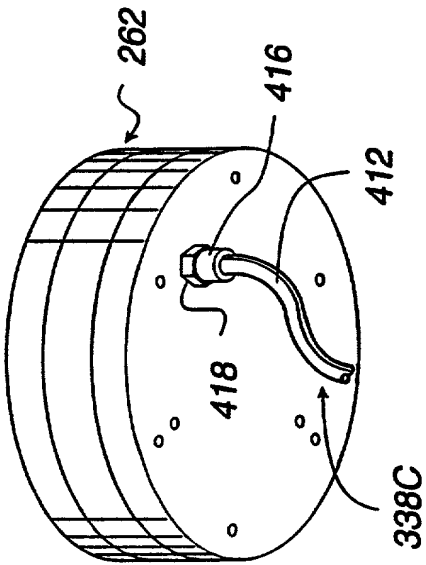


FIG. 5A-3

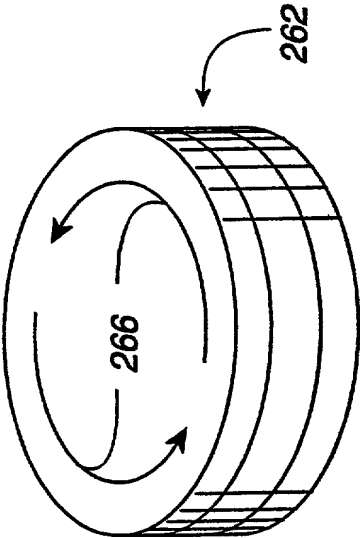


FIG. 5B-3

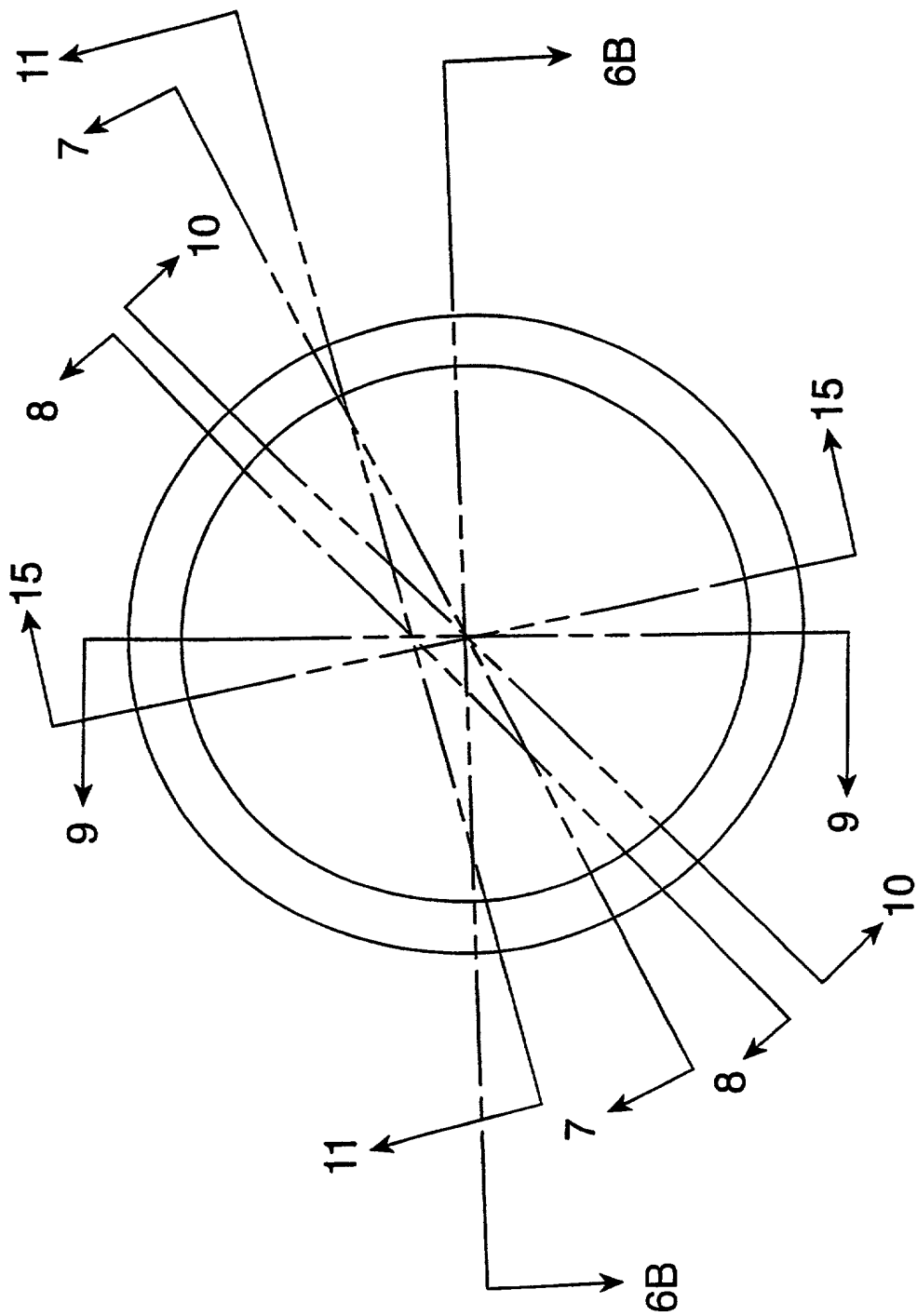


FIG. 6A

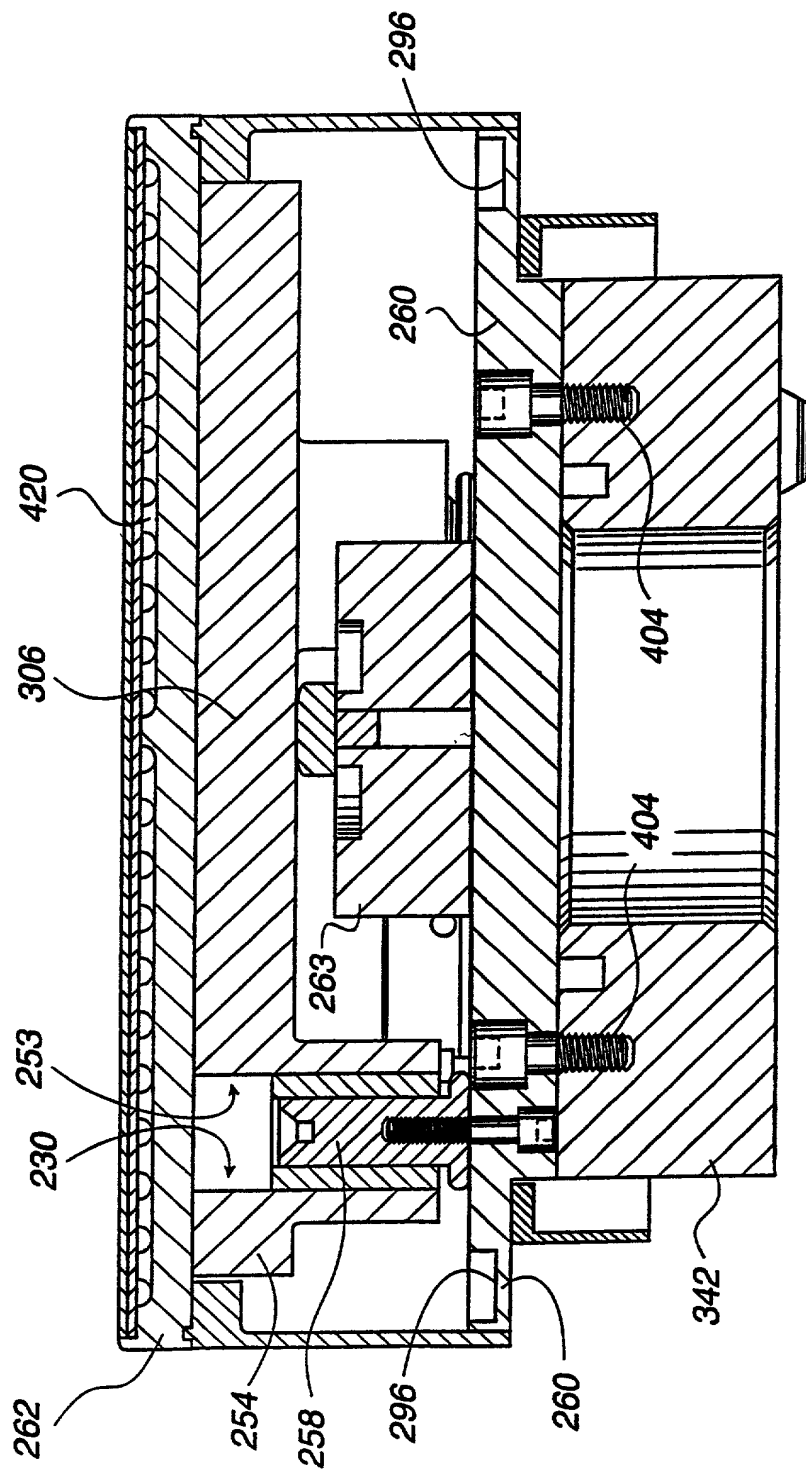


FIG. 6B

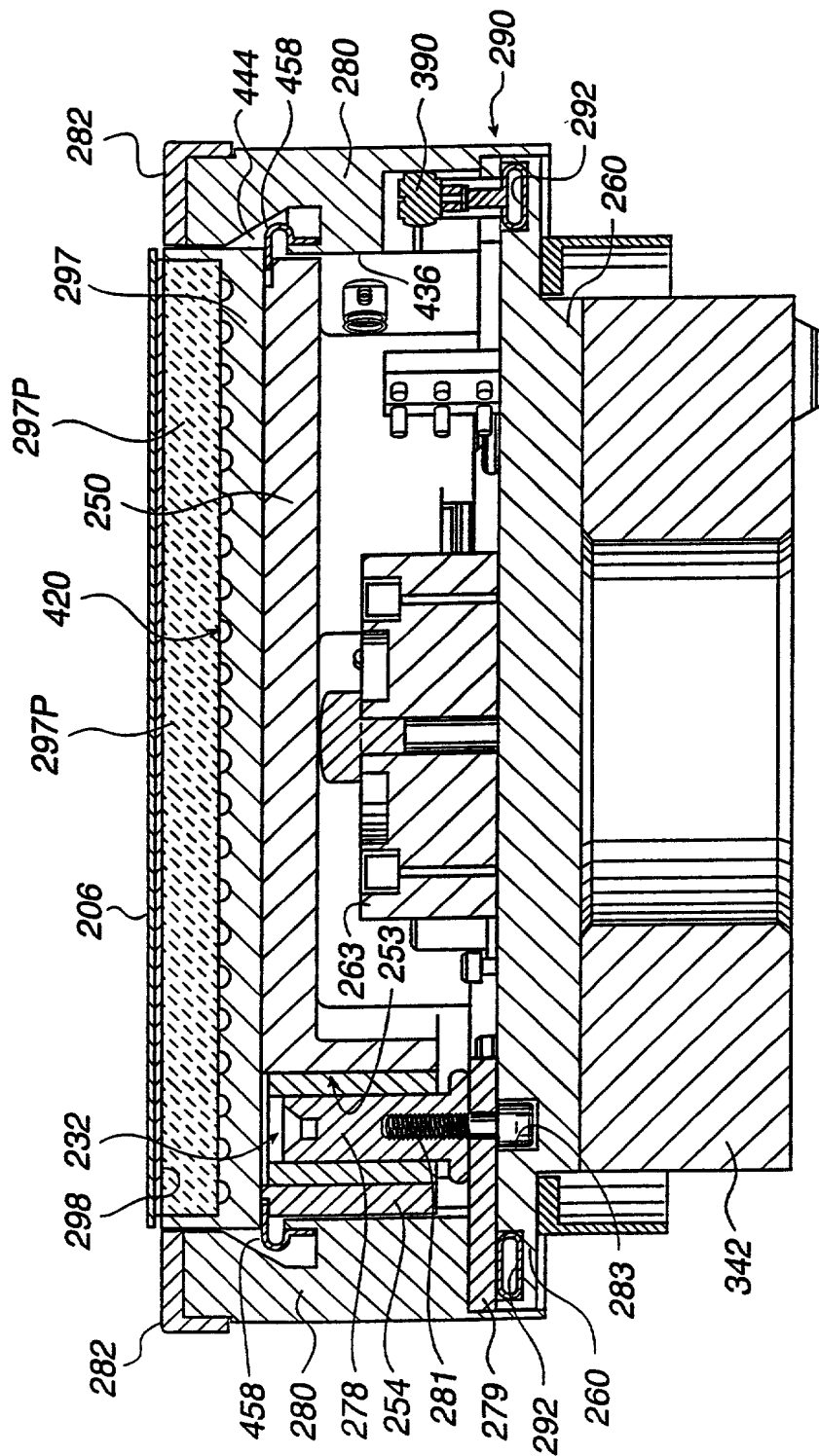
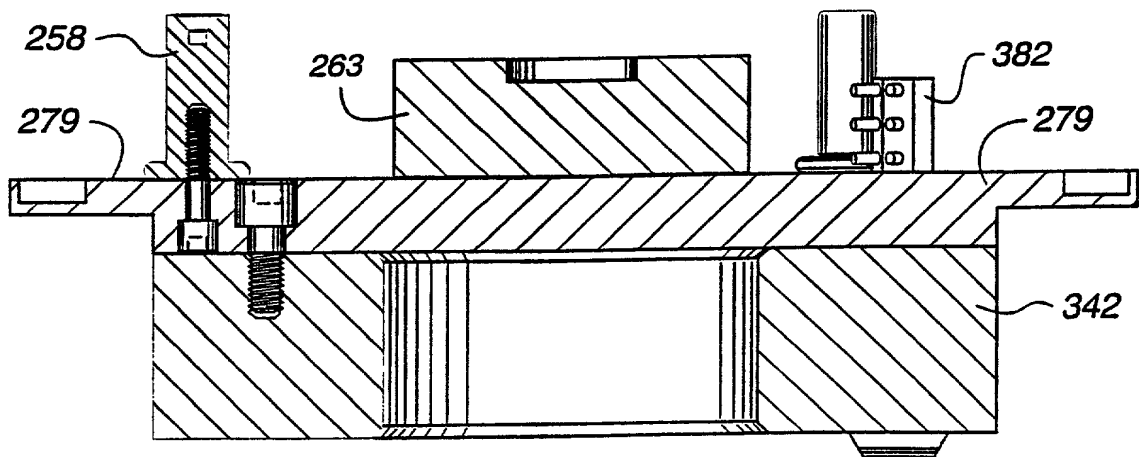
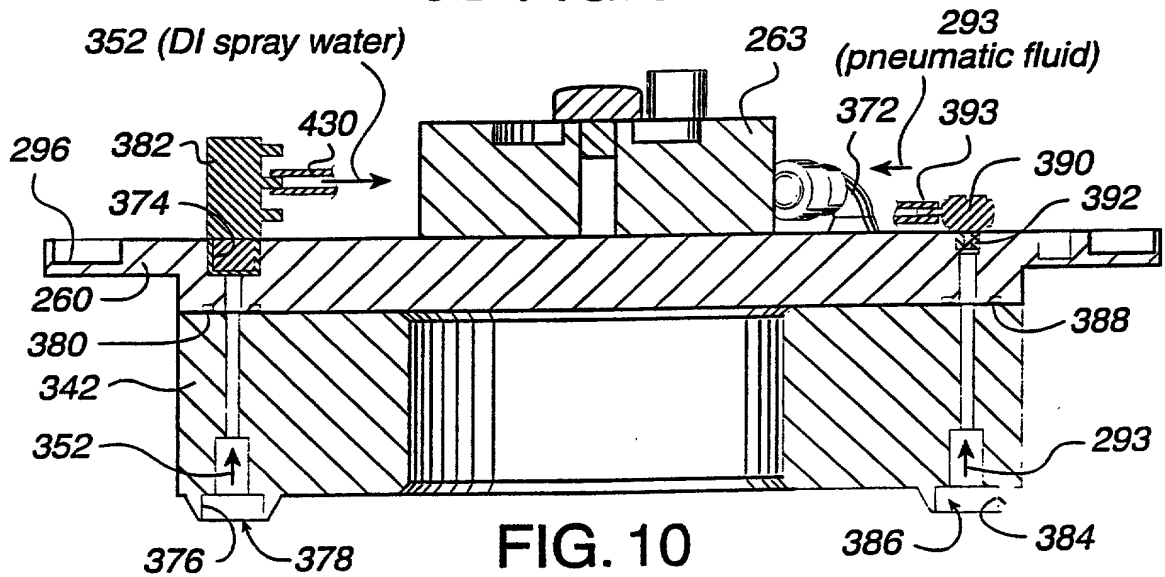
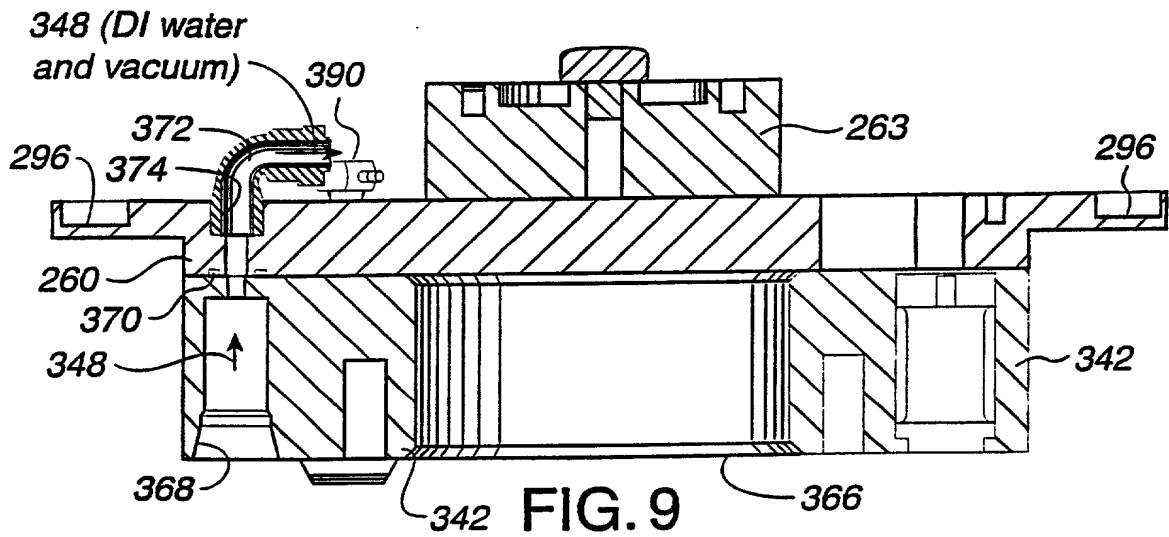


FIG. 7



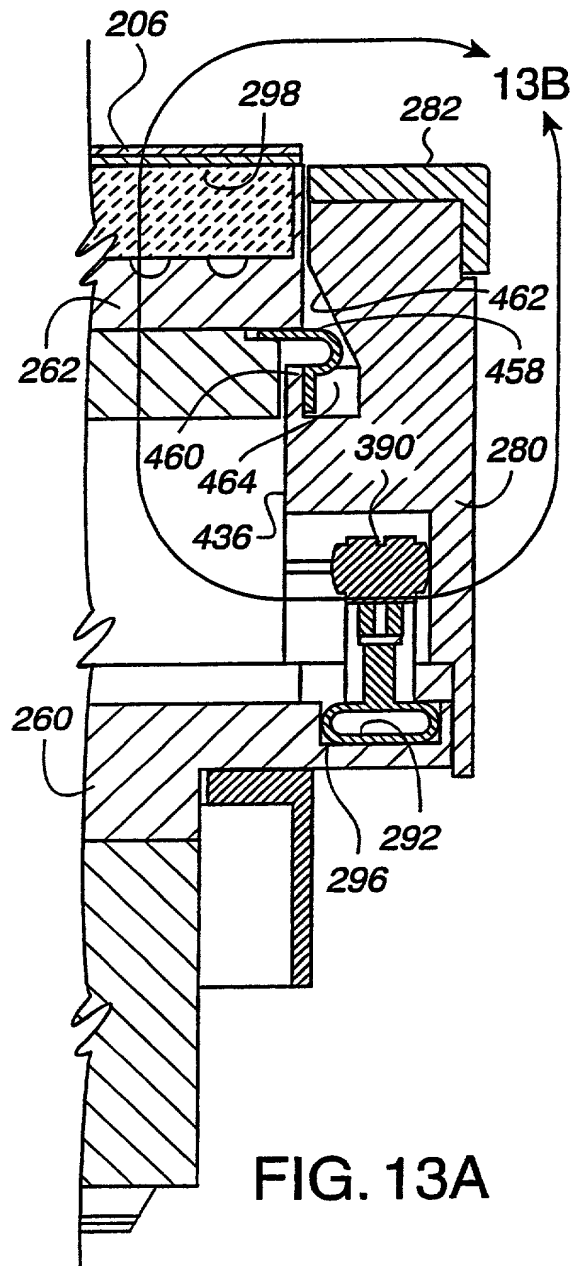
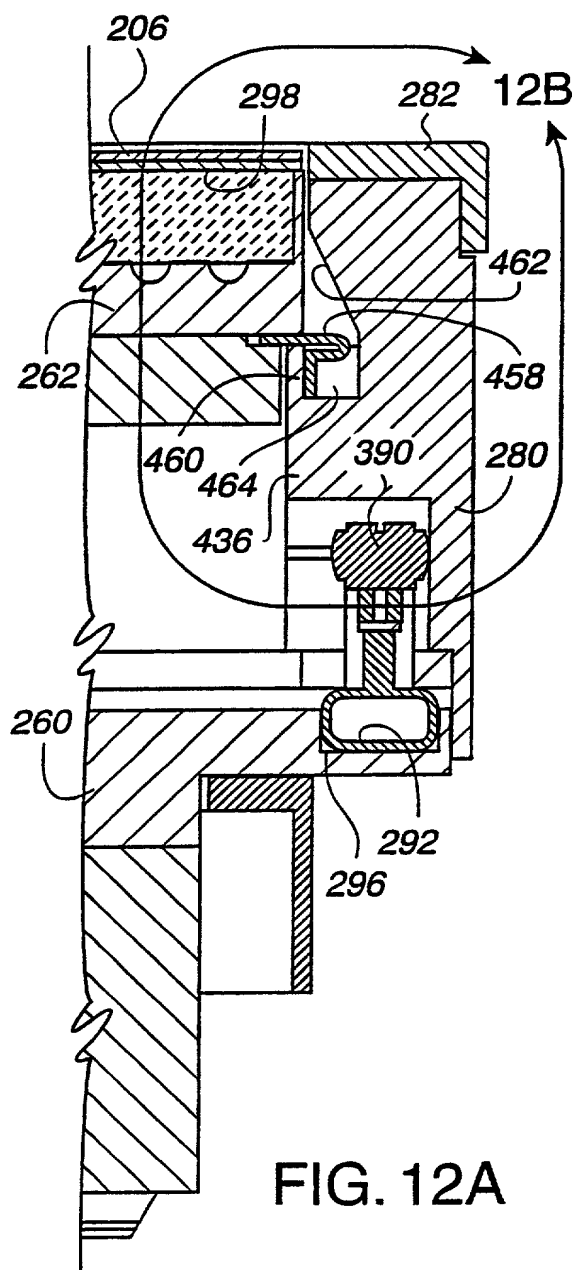


FIG. 12B is a cross-sectional view of the device 100 taken along line 12-12 of FIG. 12A. The device 100 includes a substrate 250, a first layer 262, a second layer 280, and a third layer 282. A first opening 206 is formed in the first layer 262, and a second opening 298 is formed in the second layer 280. A first conductive layer 436 is disposed on the first layer 262, and a second conductive layer 458 is disposed on the second layer 280. A third conductive layer 462 is disposed on the third layer 282. The first conductive layer 436 is electrically connected to the second conductive layer 458, and the second conductive layer 458 is electrically connected to the third conductive layer 462. The first conductive layer 436 is also electrically connected to a first terminal 436, and the second conductive layer 458 is also electrically connected to a second terminal 458. The third conductive layer 462 is also electrically connected to a third terminal 462.

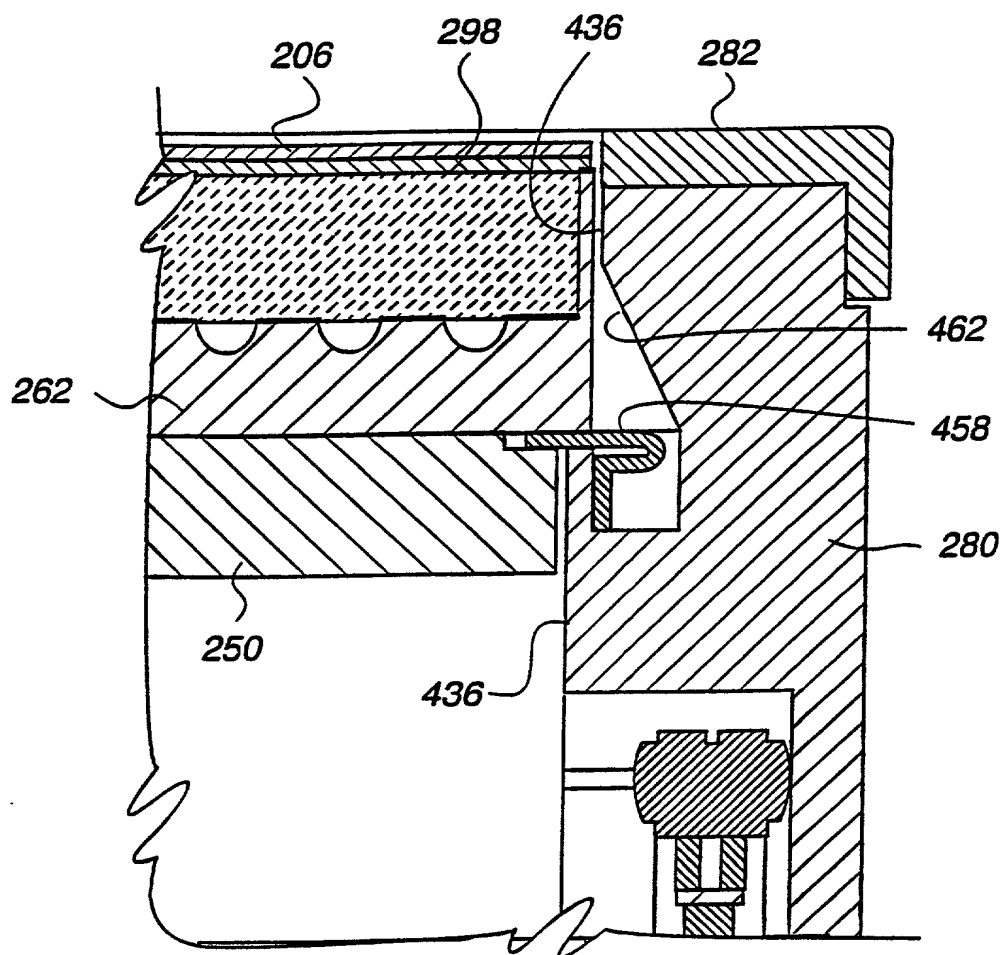


FIG. 12B

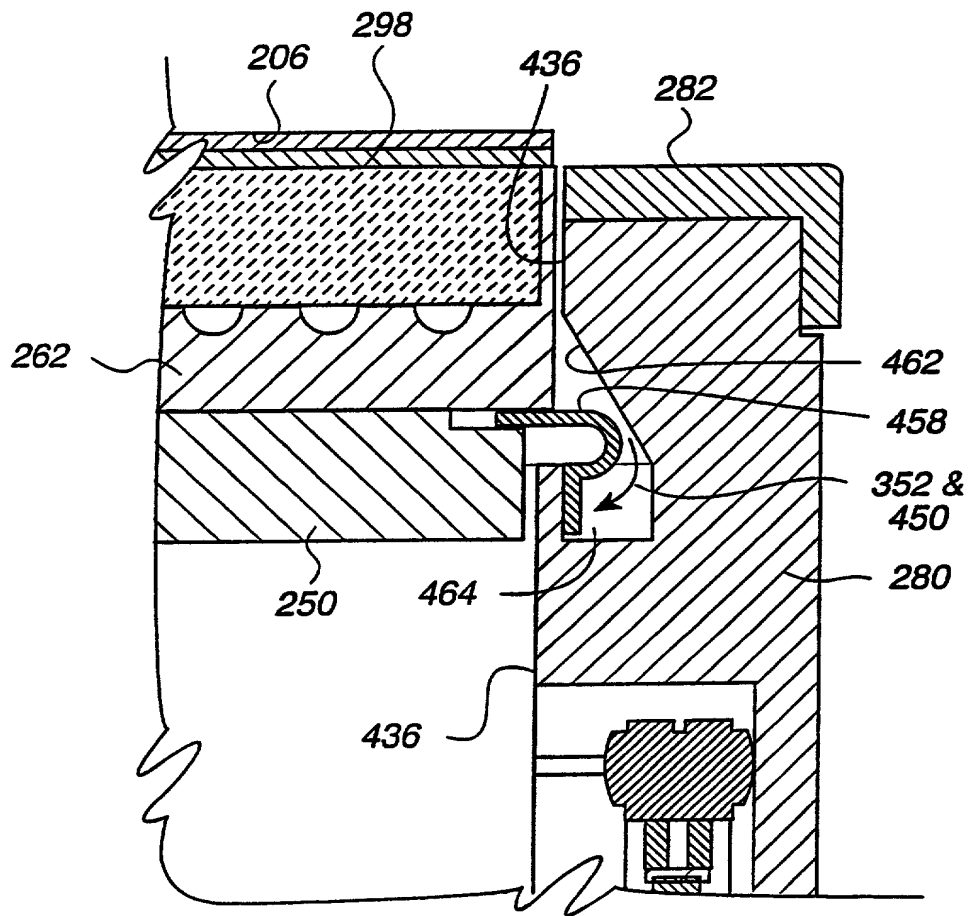
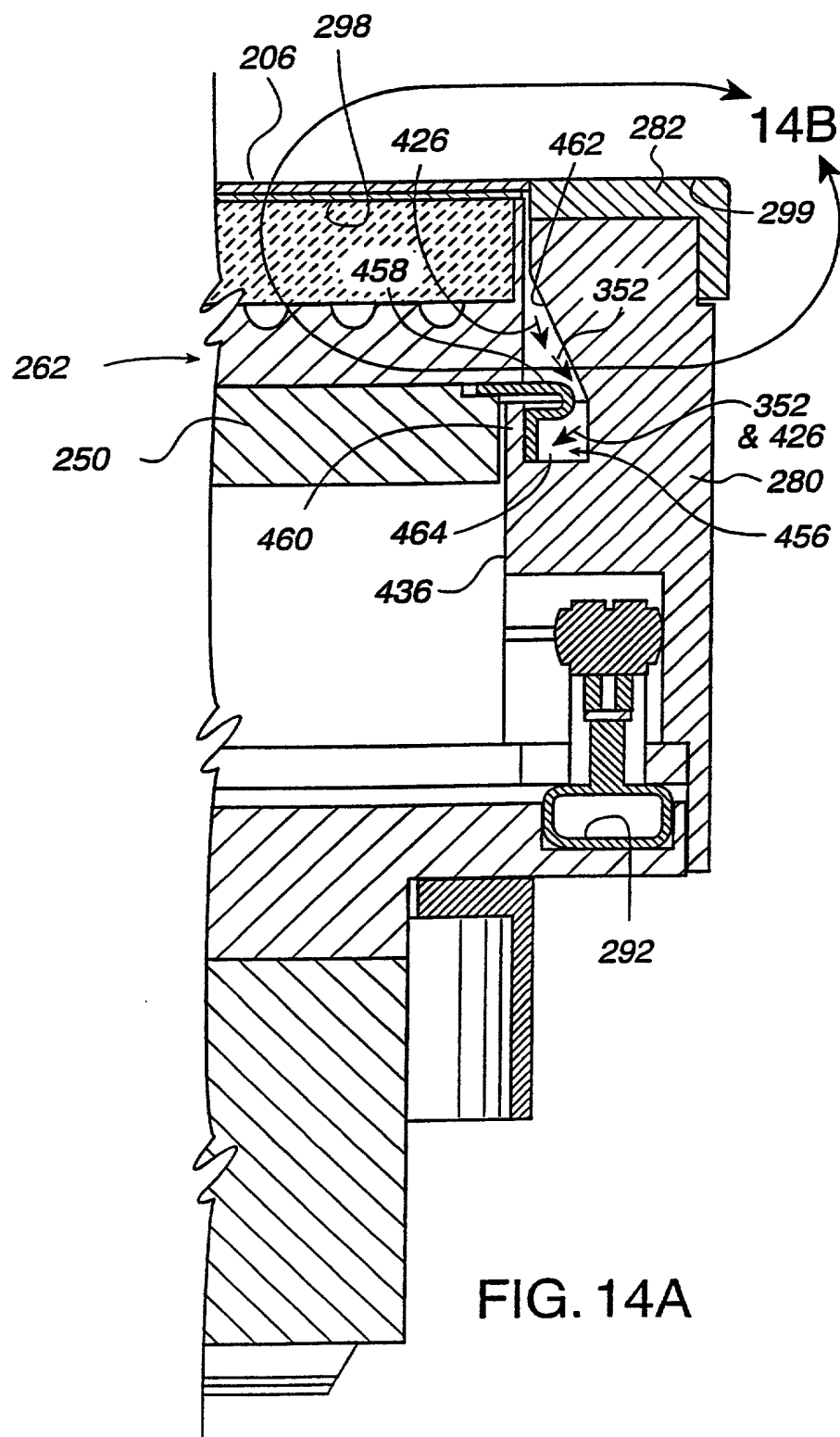


FIG. 13B



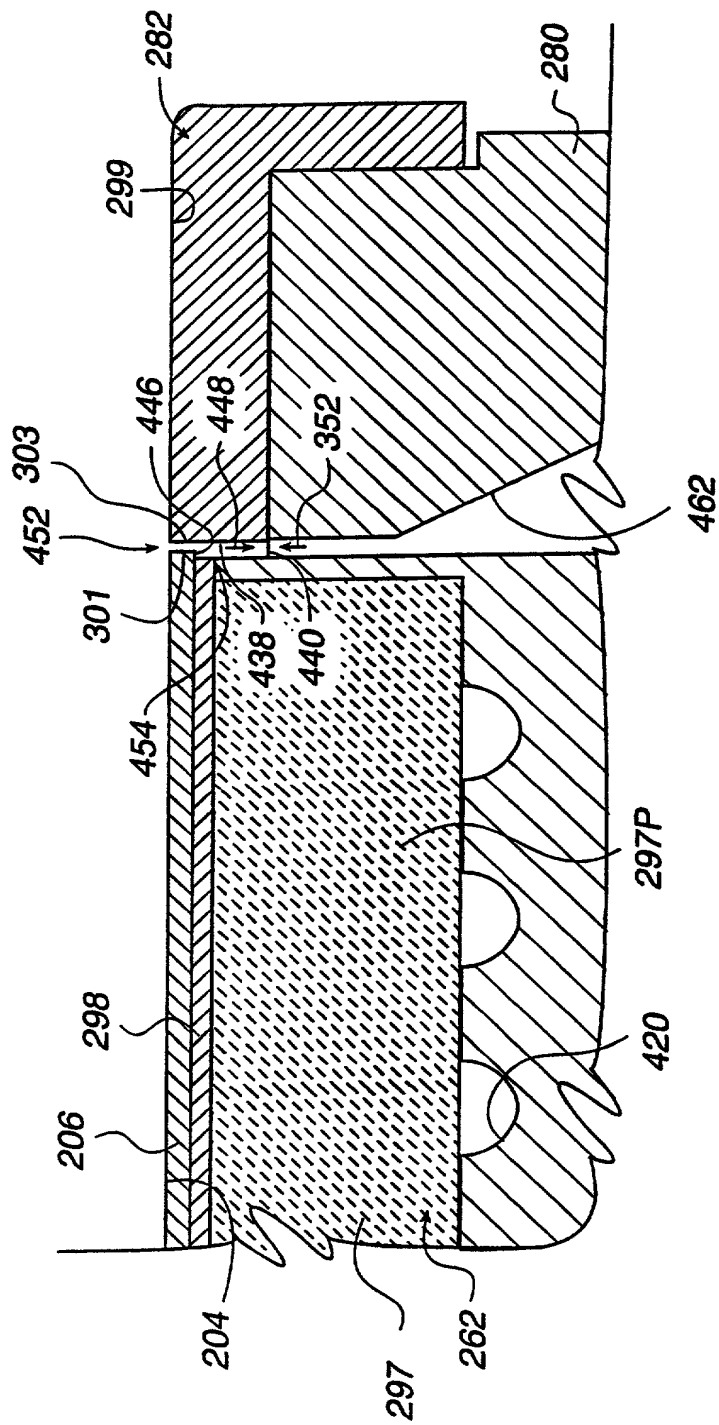


FIG. 14B

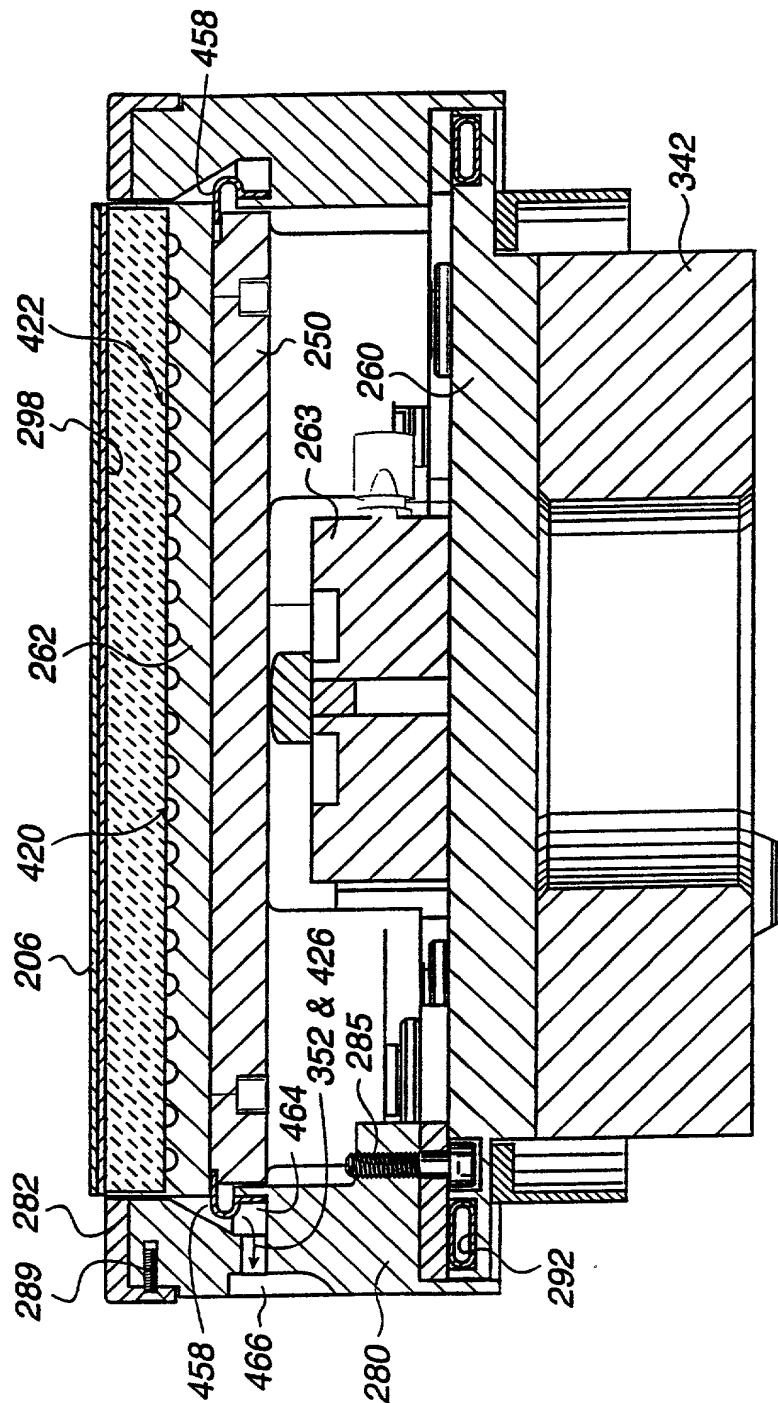


FIG. 15

FIG. 16B

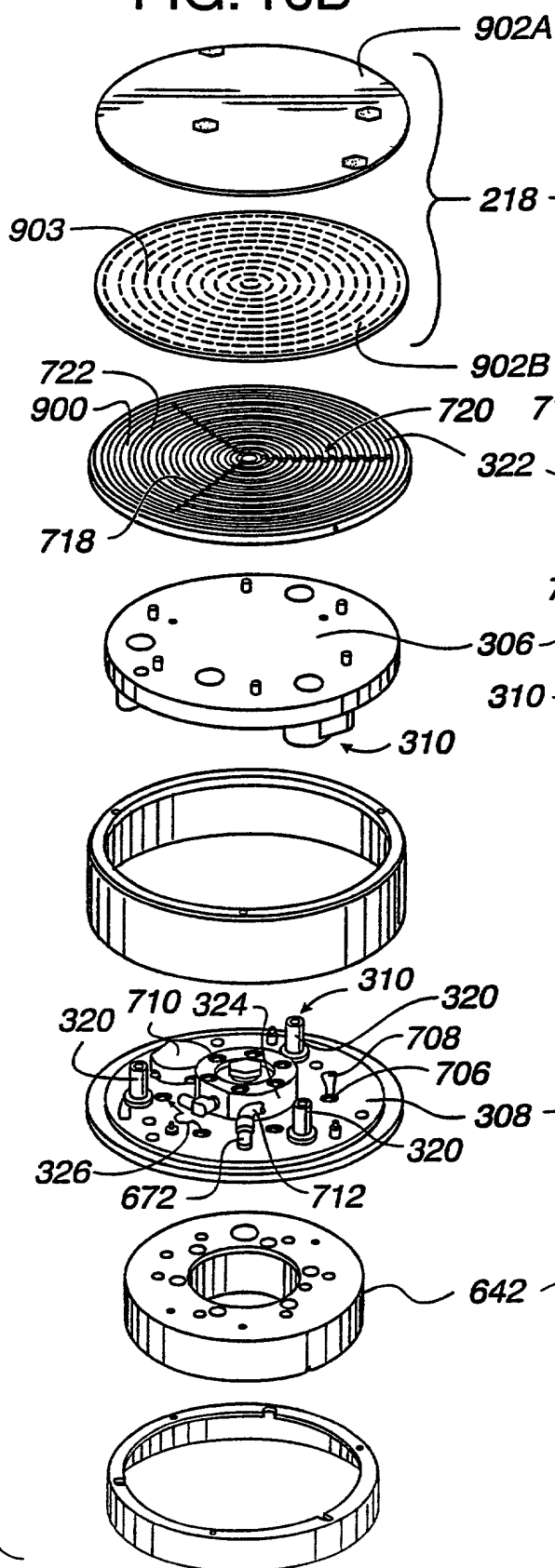
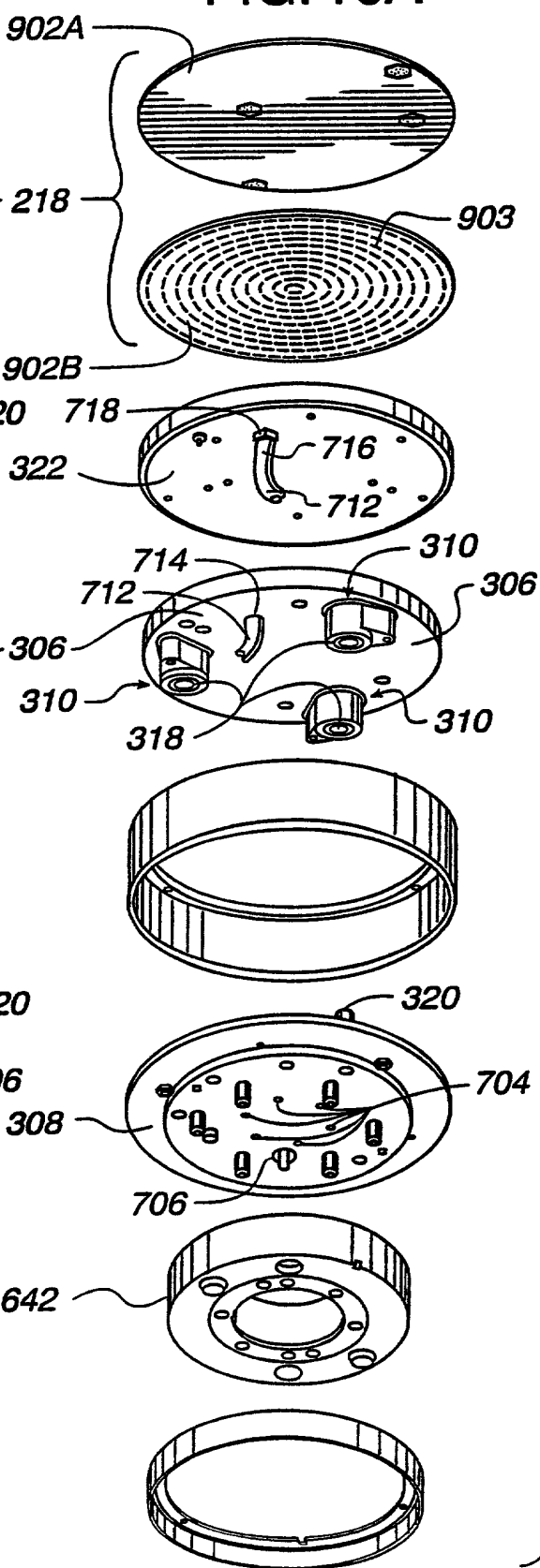


FIG. 16A



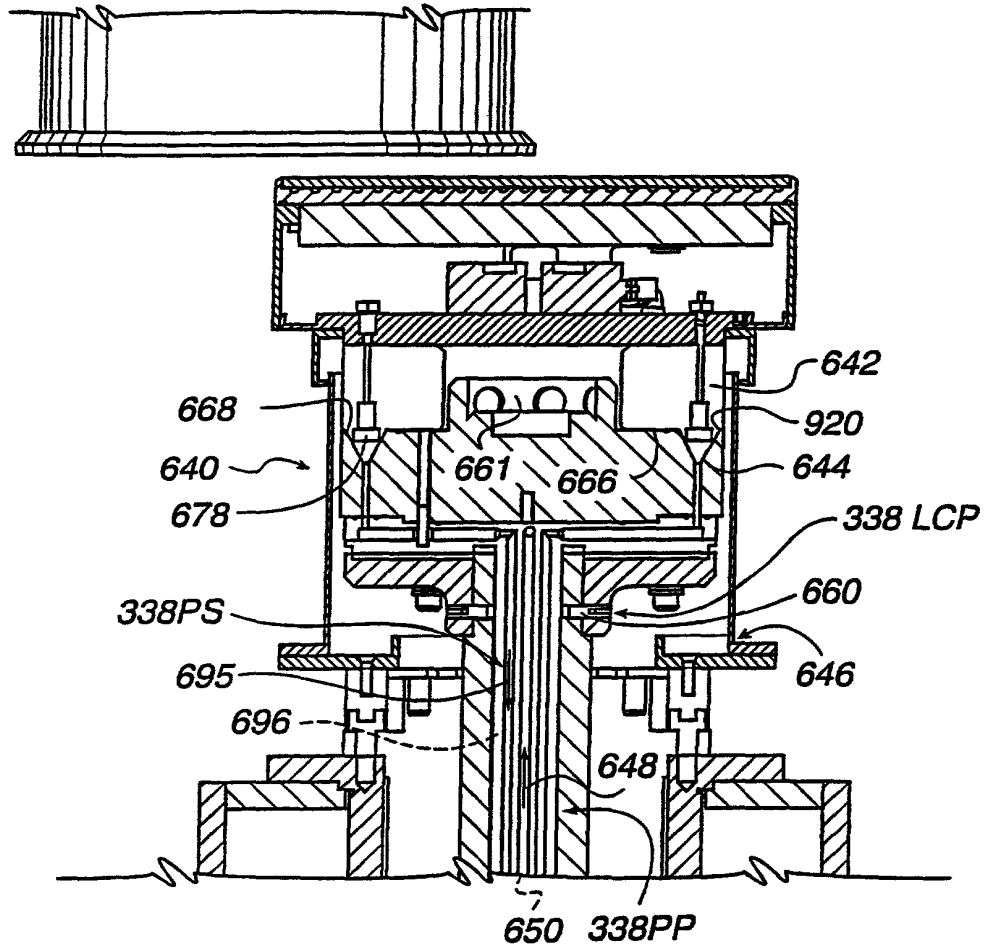


FIG. 17C

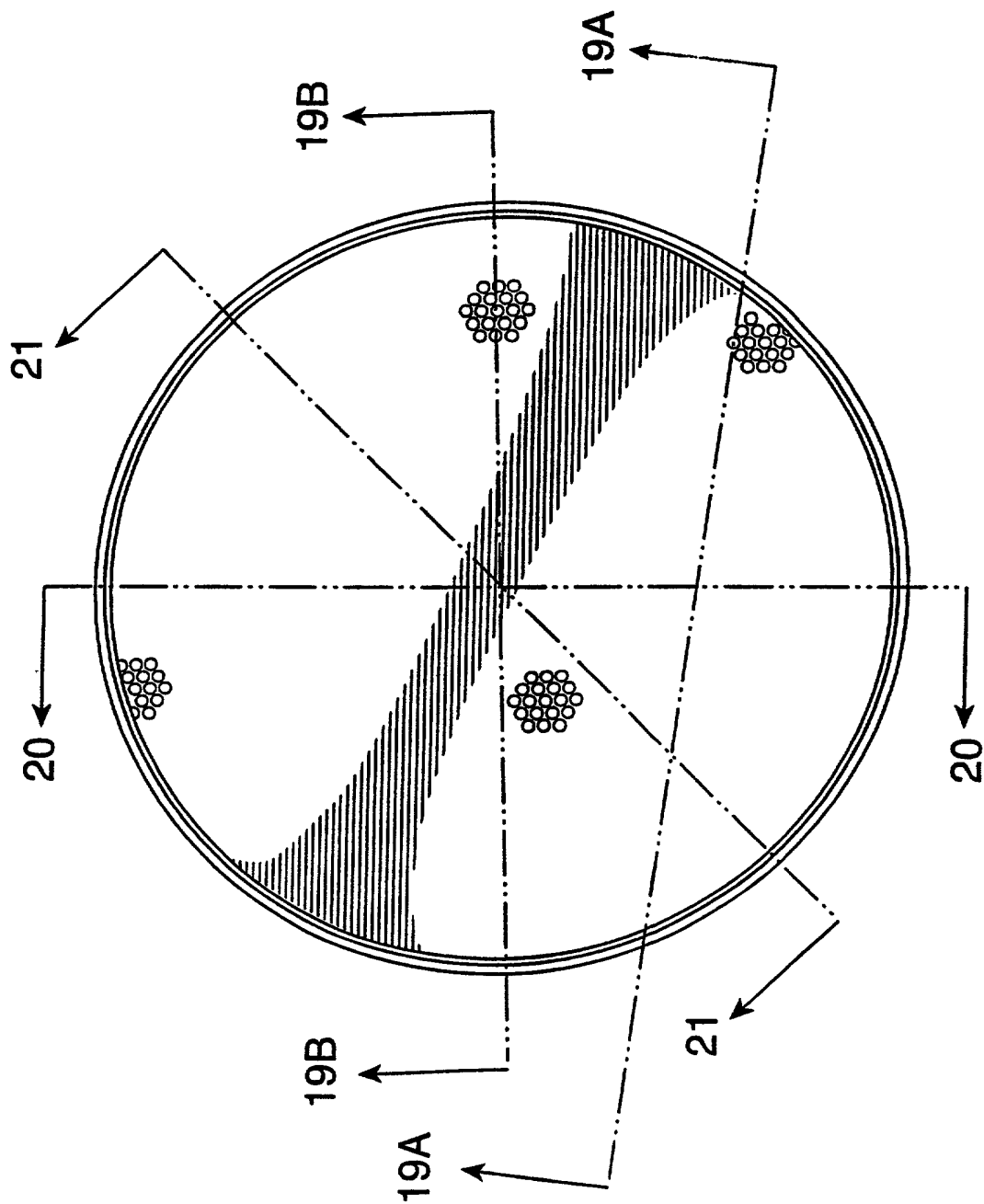


FIG. 18

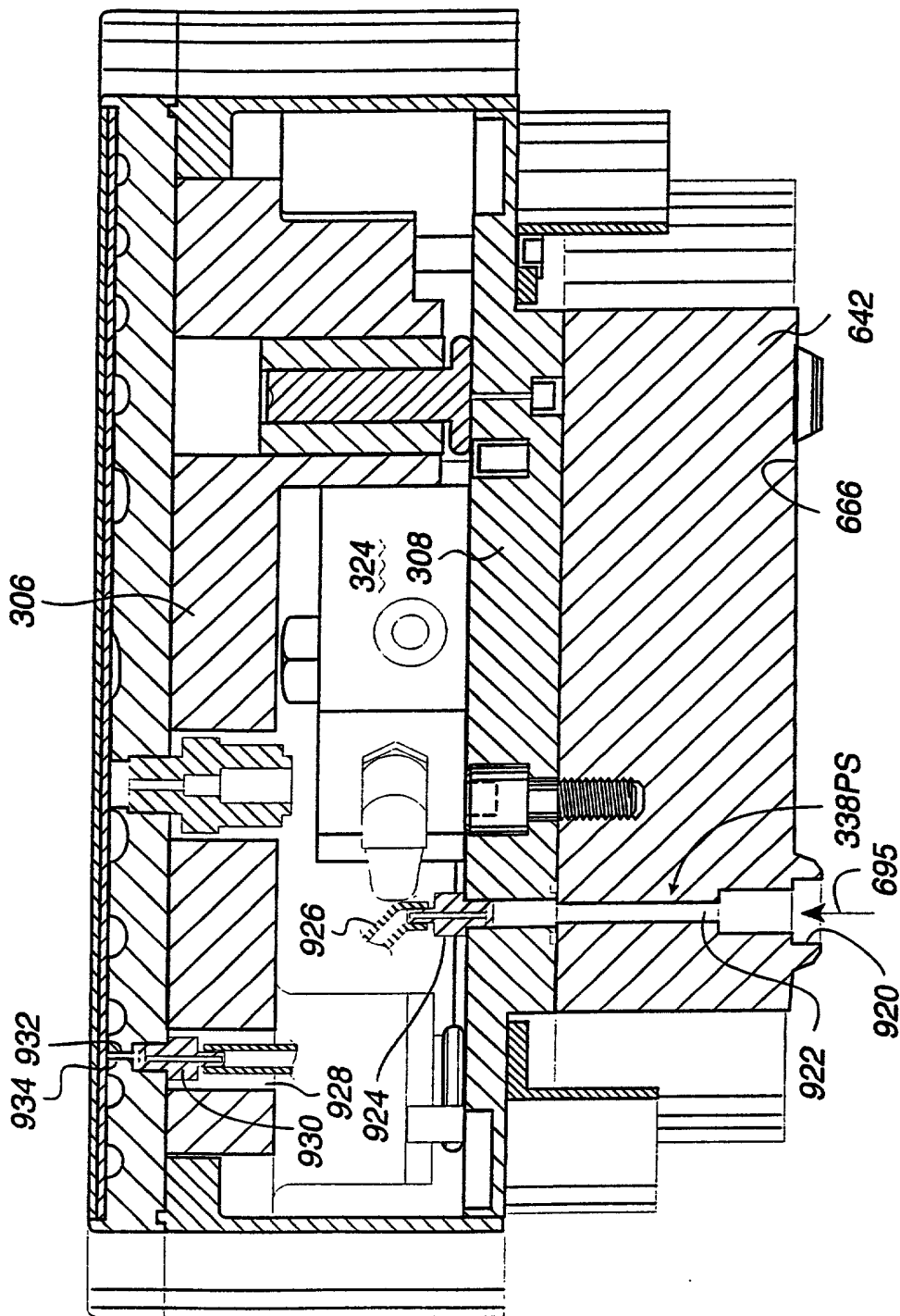


FIG. 19A

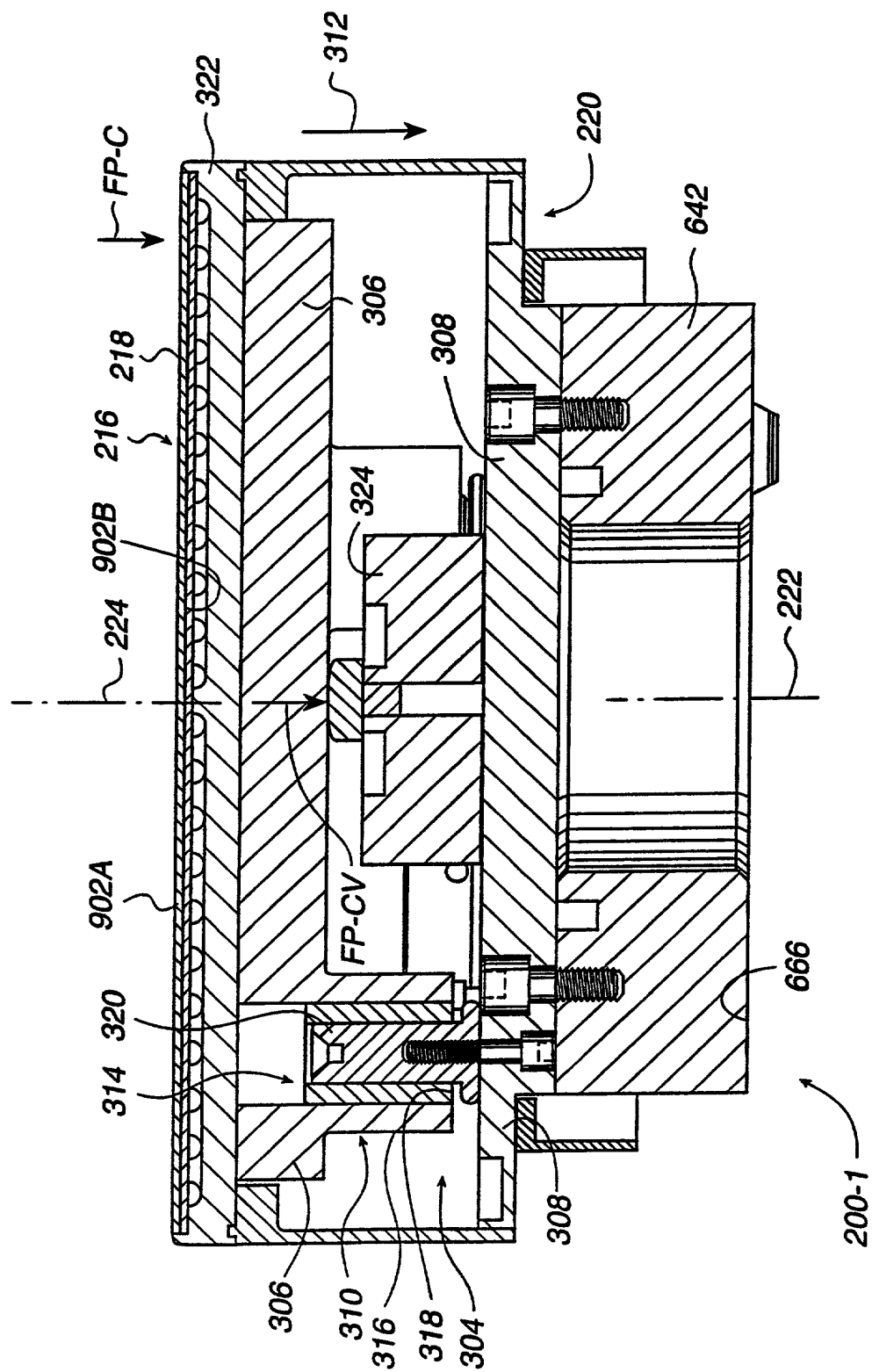


FIG. 19B

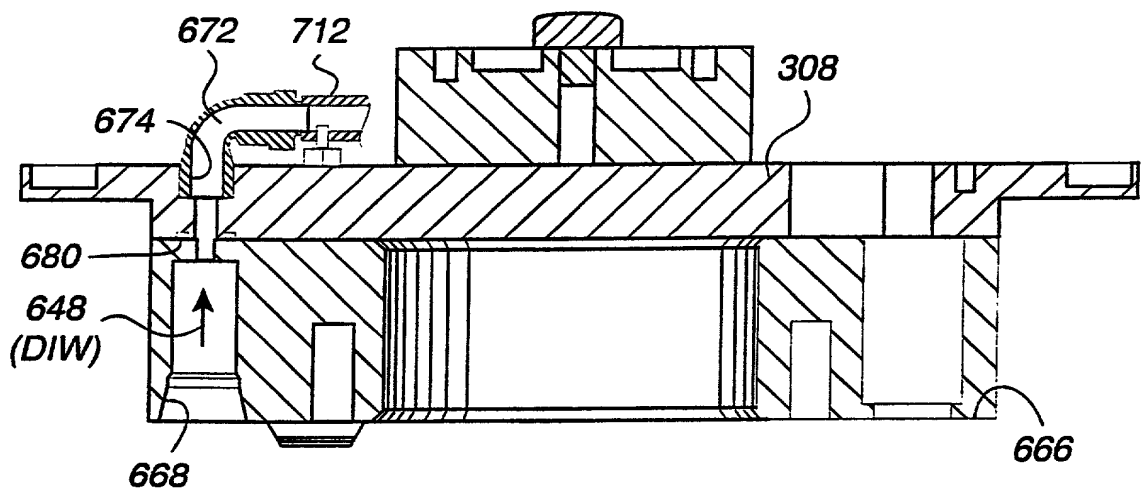


FIG. 20

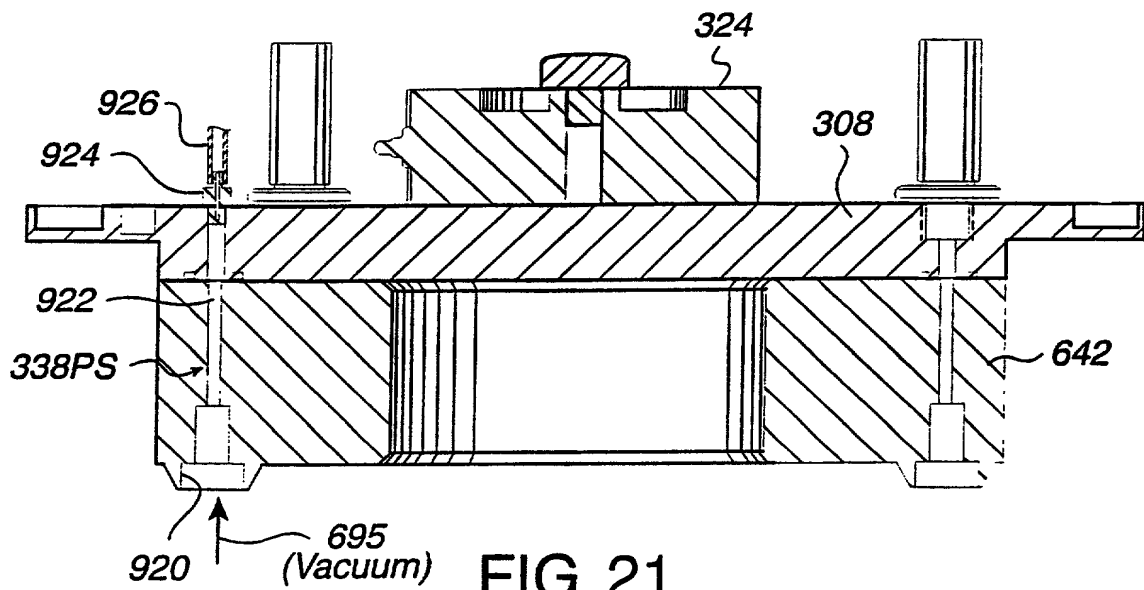


FIG. 21

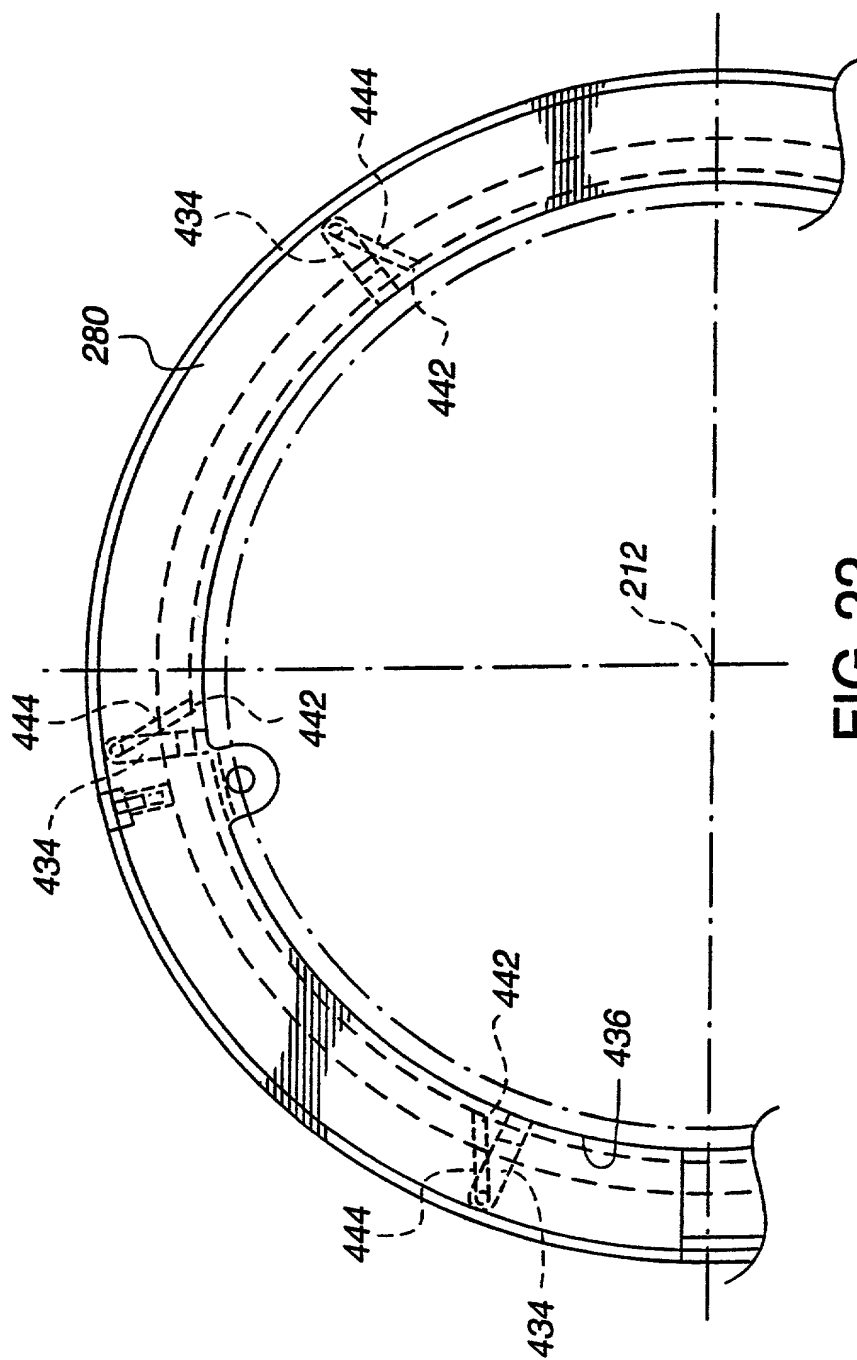


FIG. 22

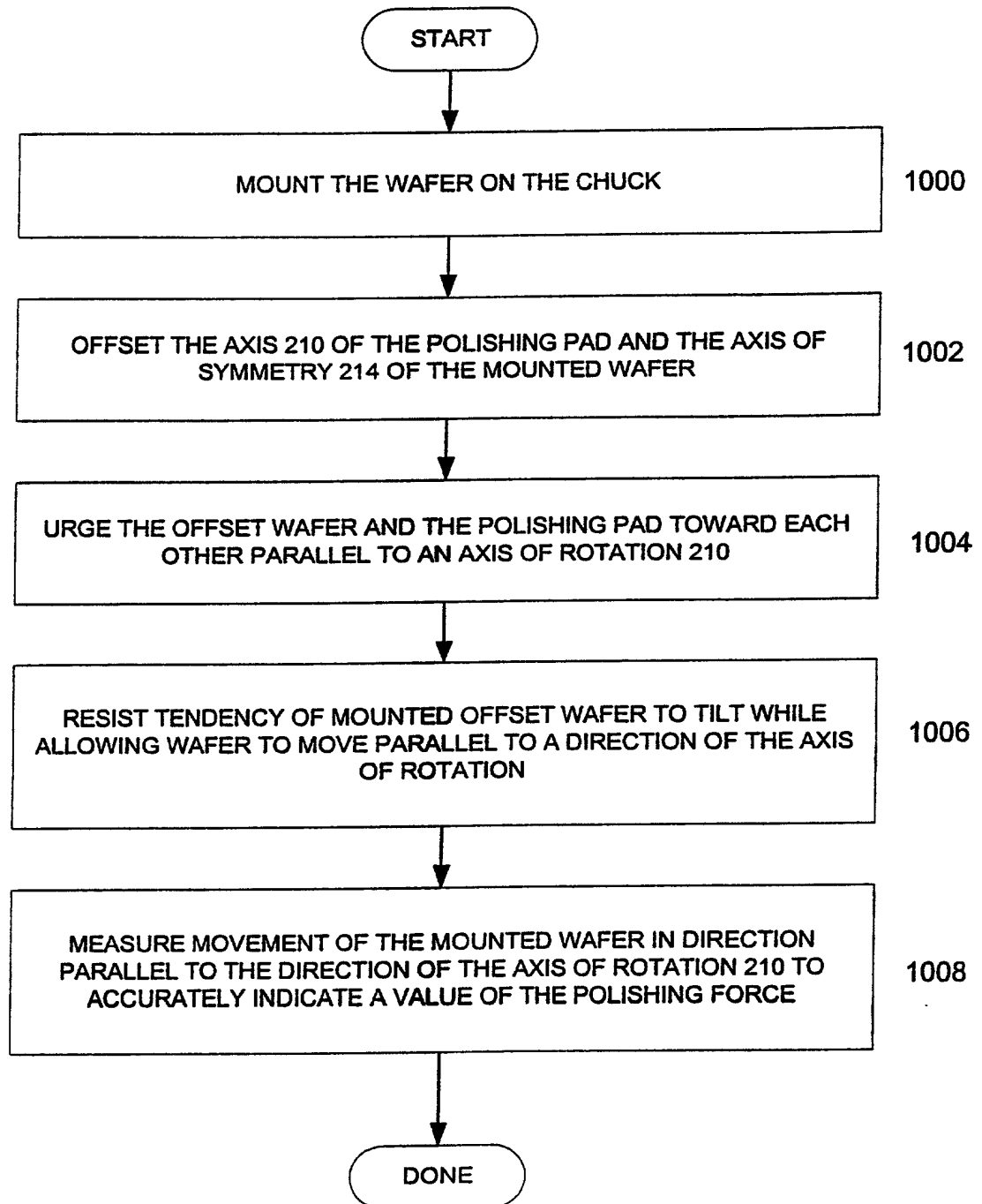


FIGURE 23

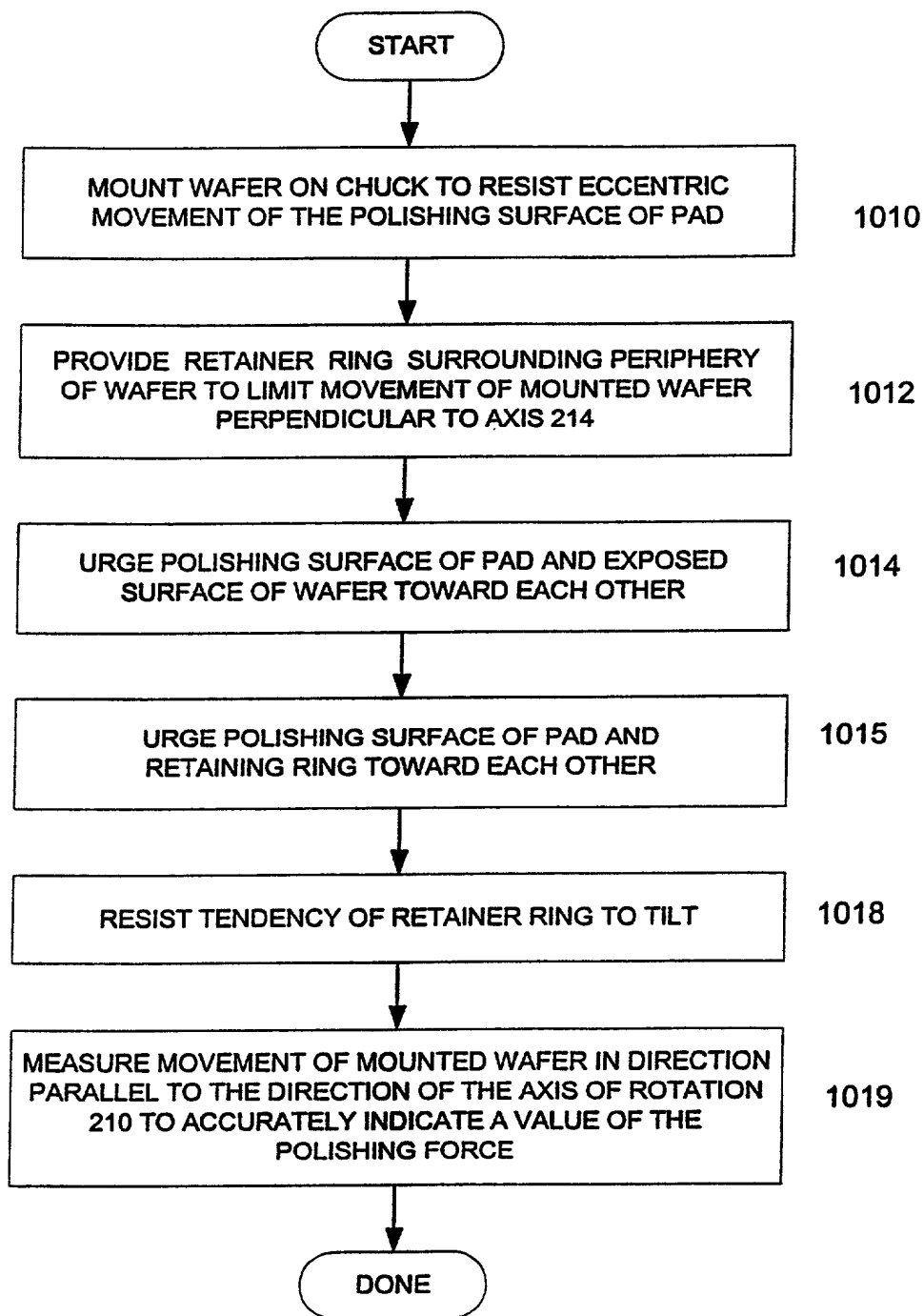


FIGURE 24

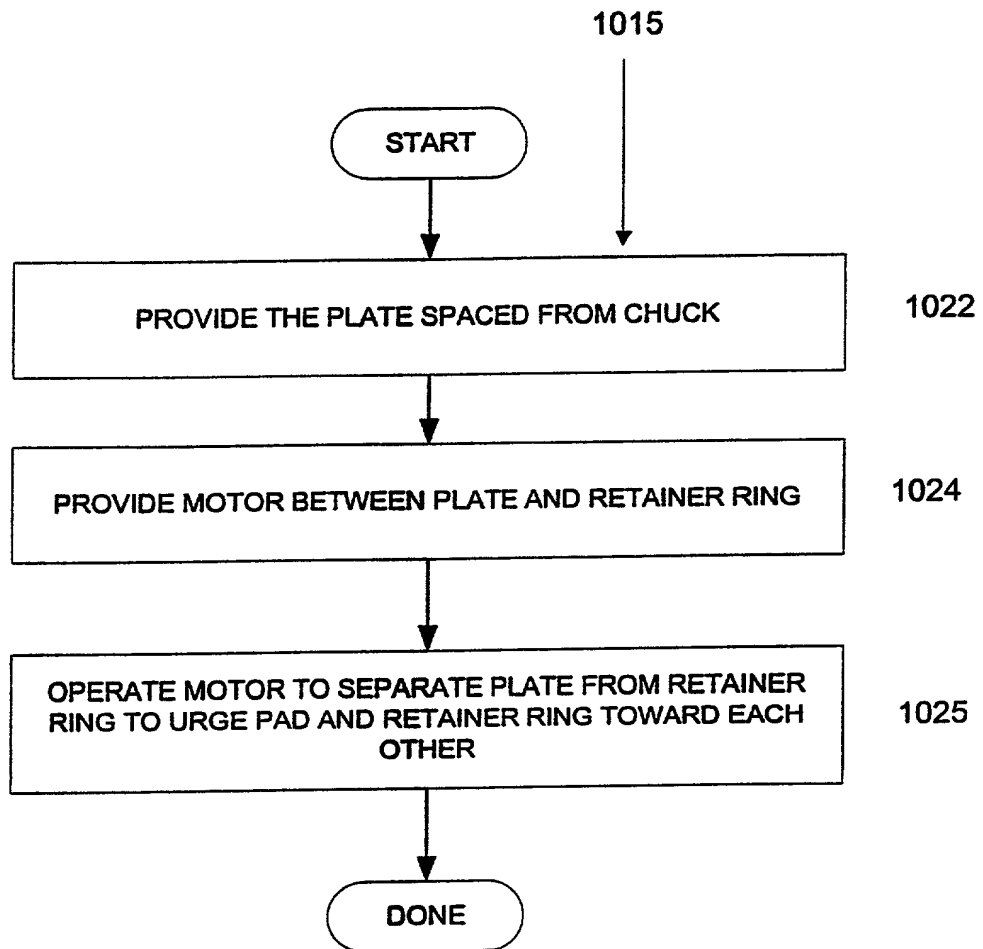


FIGURE 25

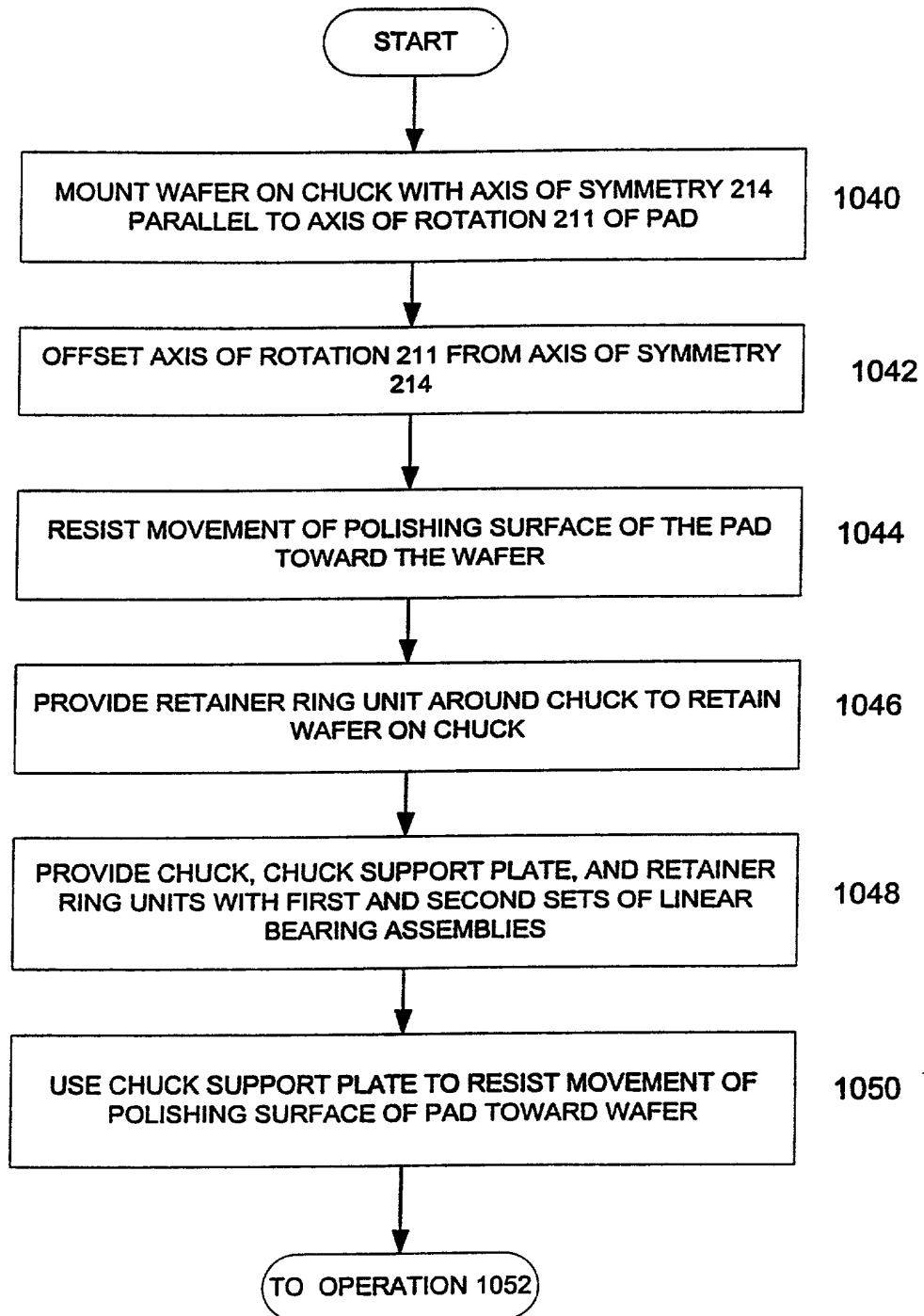


FIGURE 26

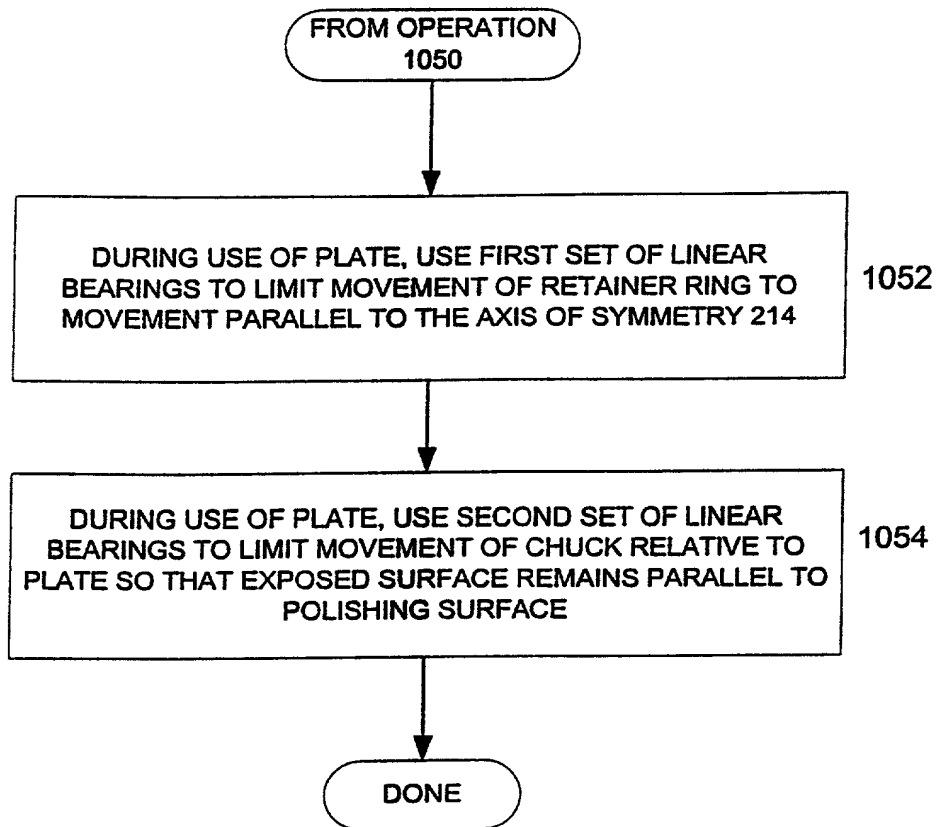


FIGURE 27

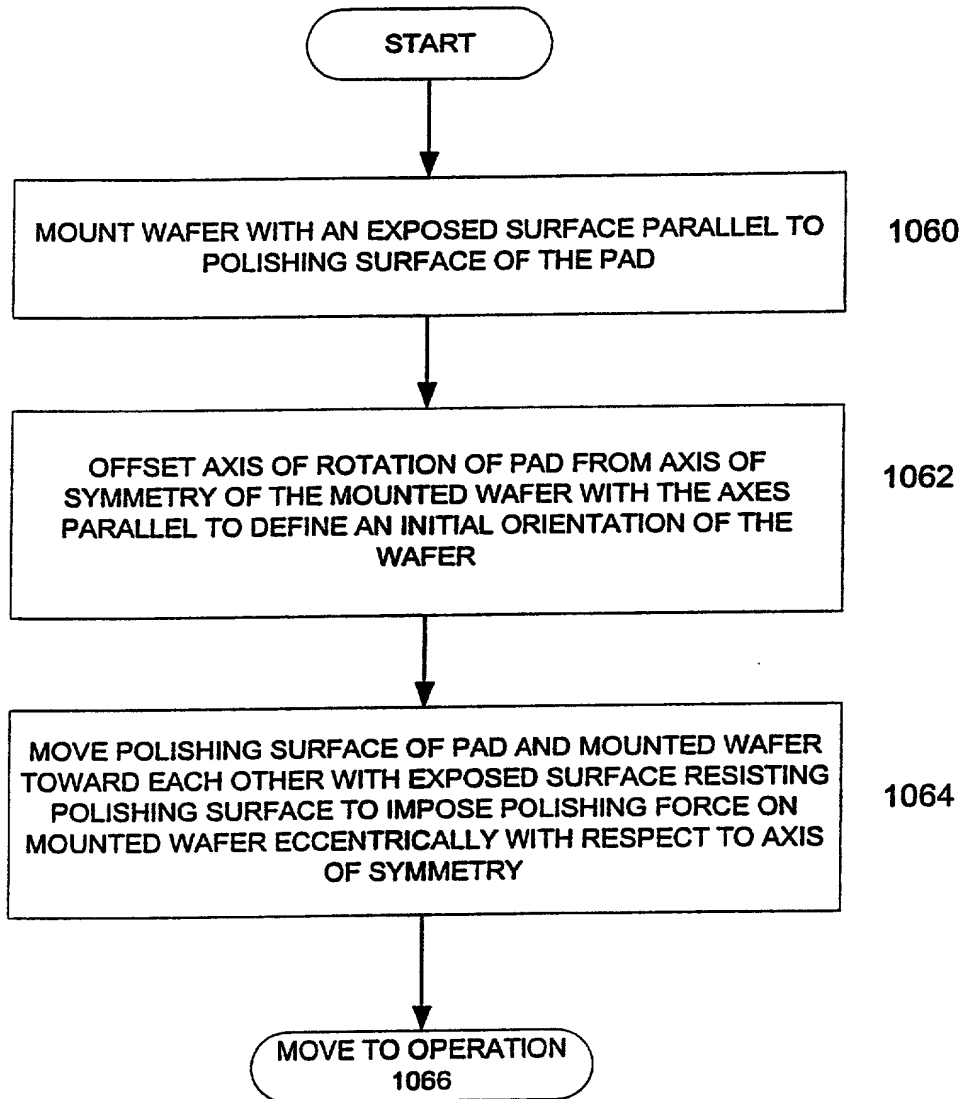


FIGURE 28

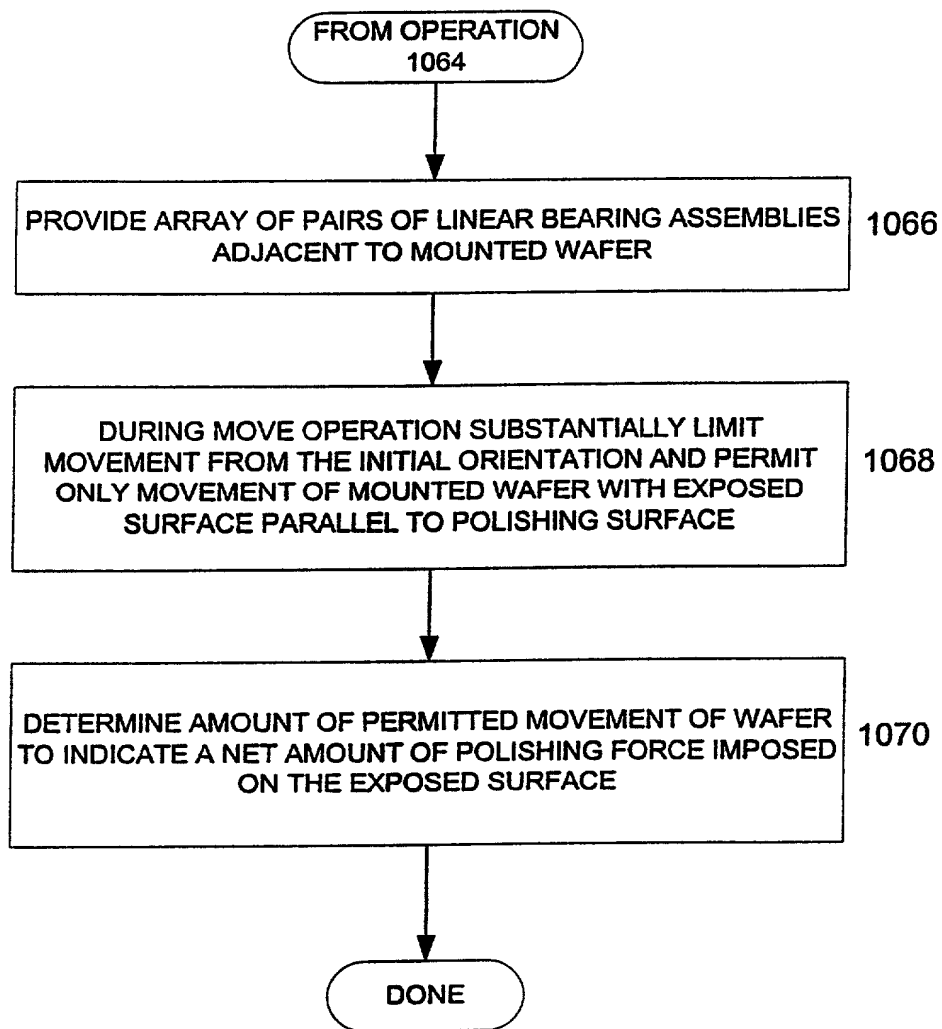


FIGURE 29

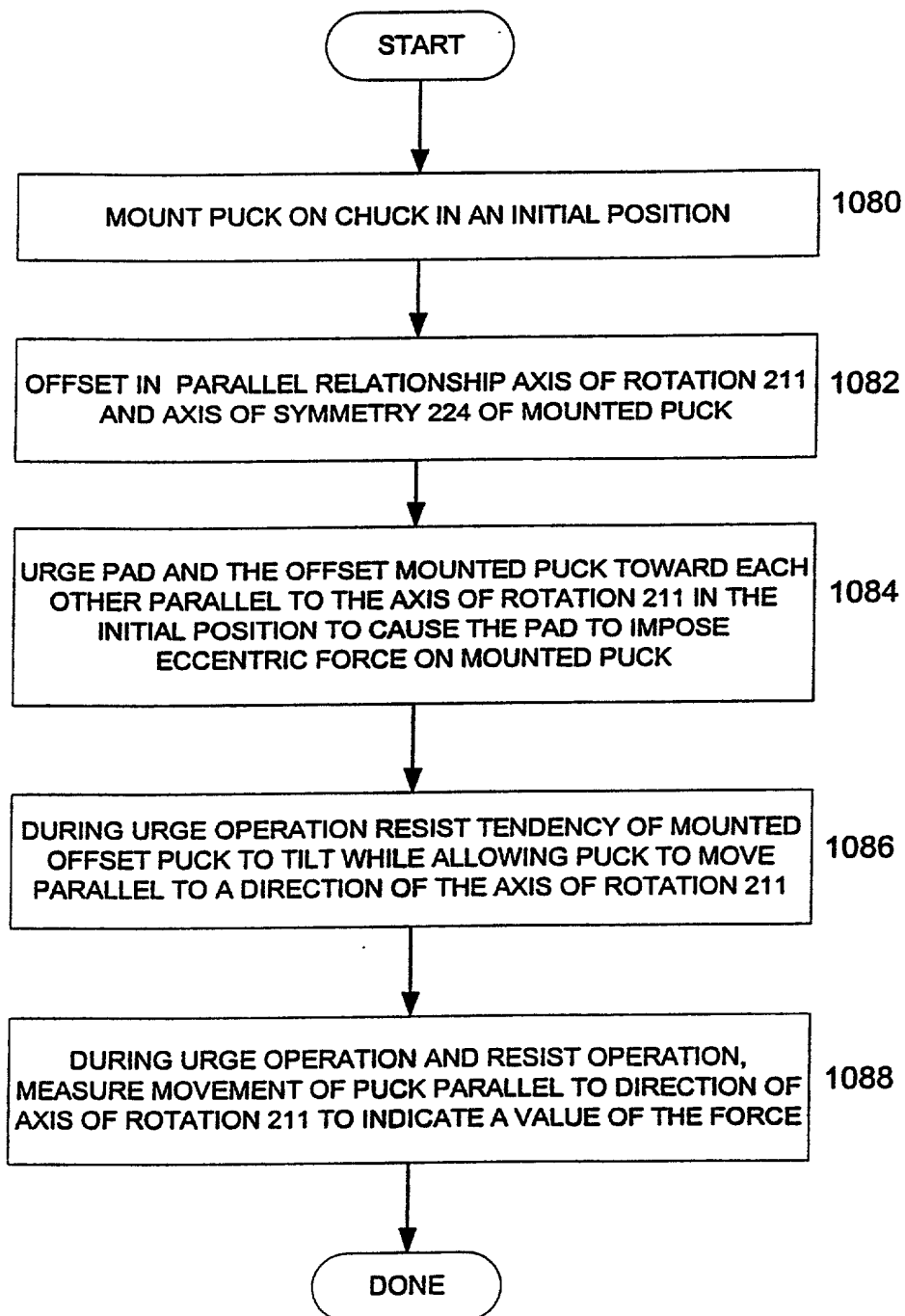


FIGURE 30

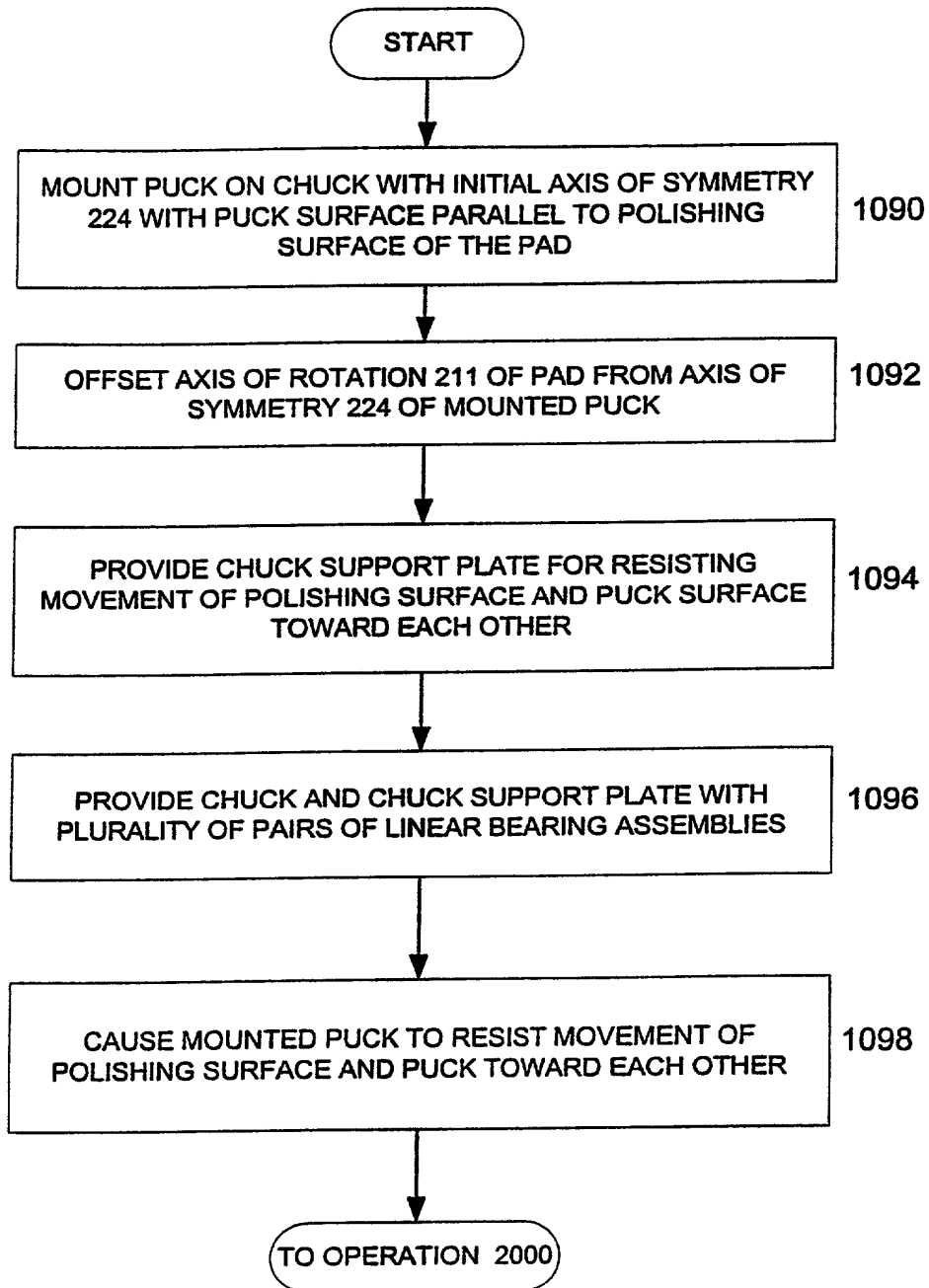


FIGURE 31

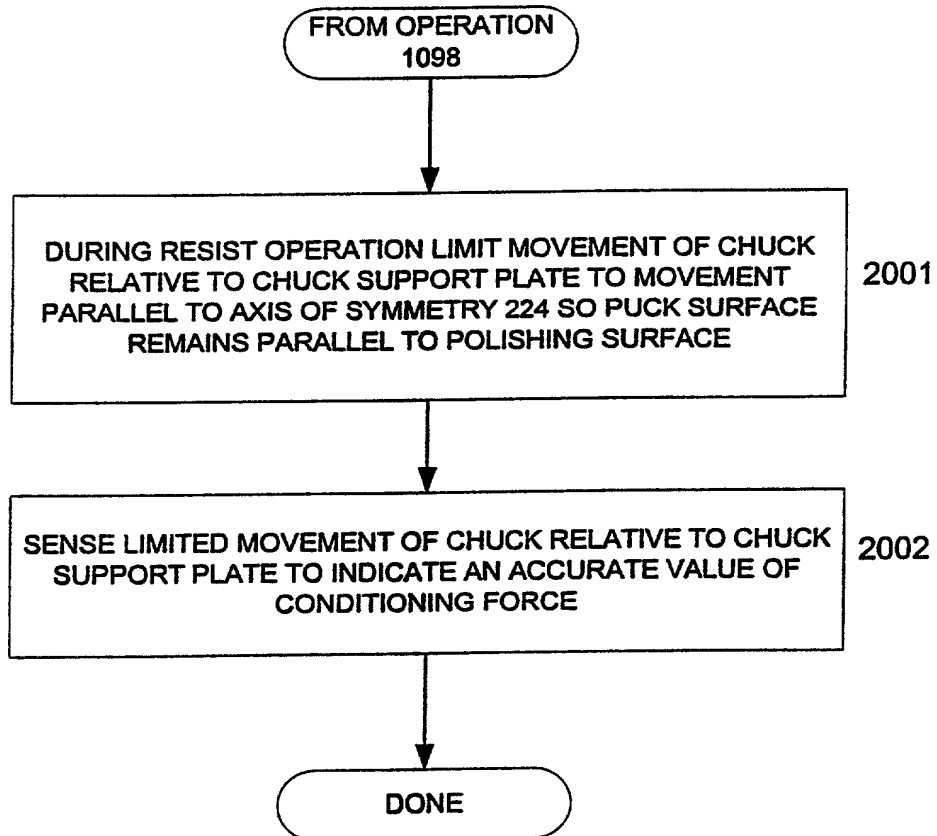


FIGURE 32

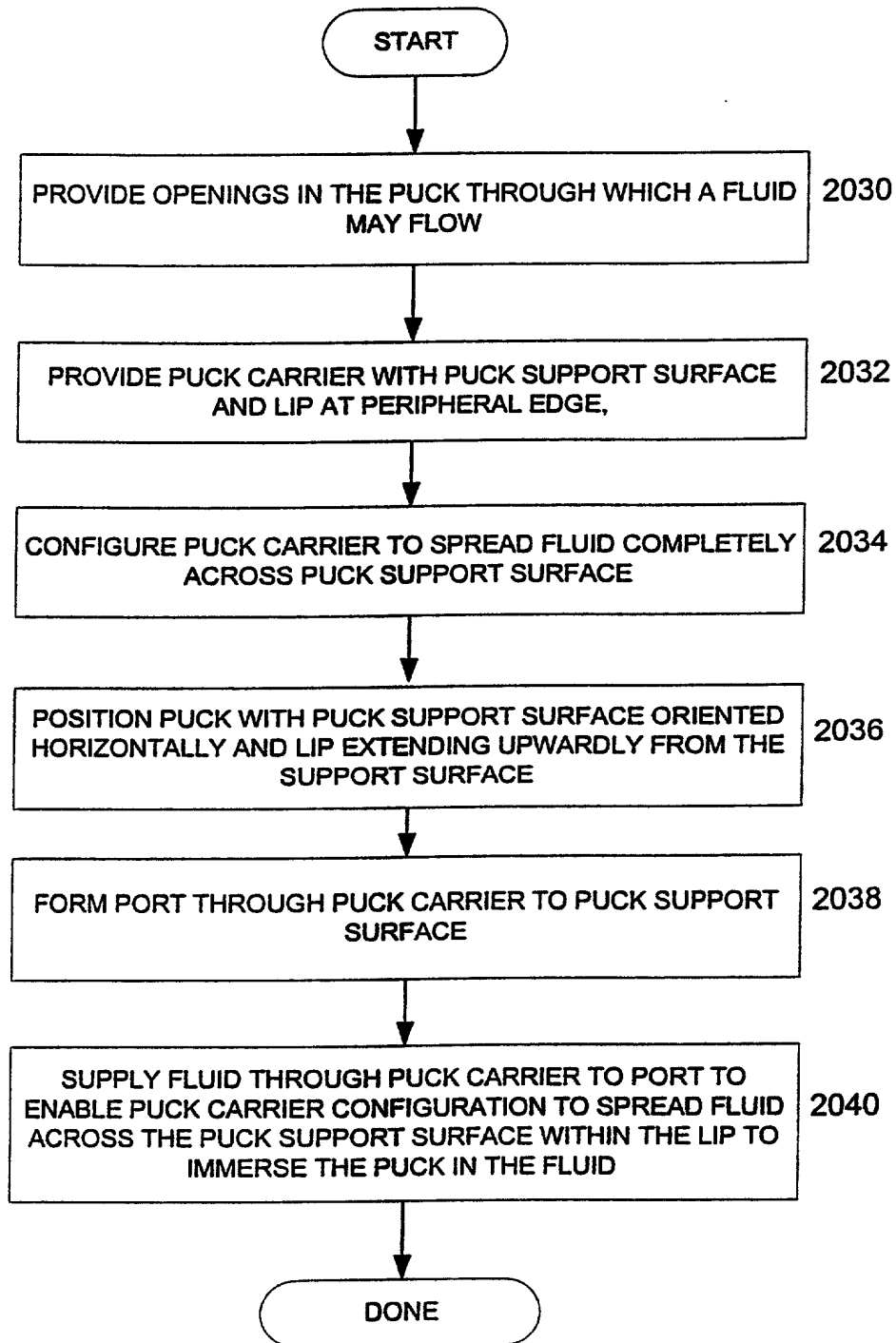


FIGURE 33

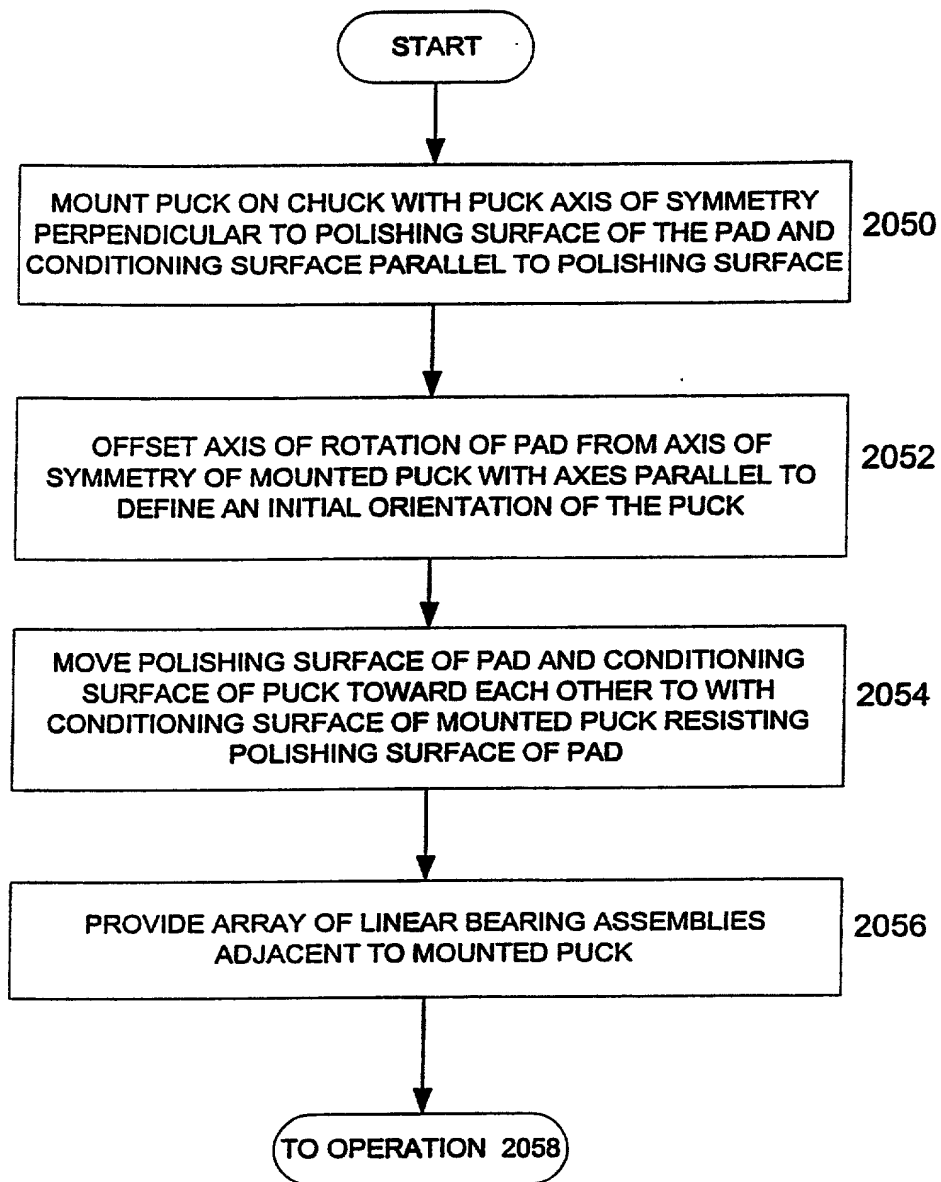


FIGURE 34

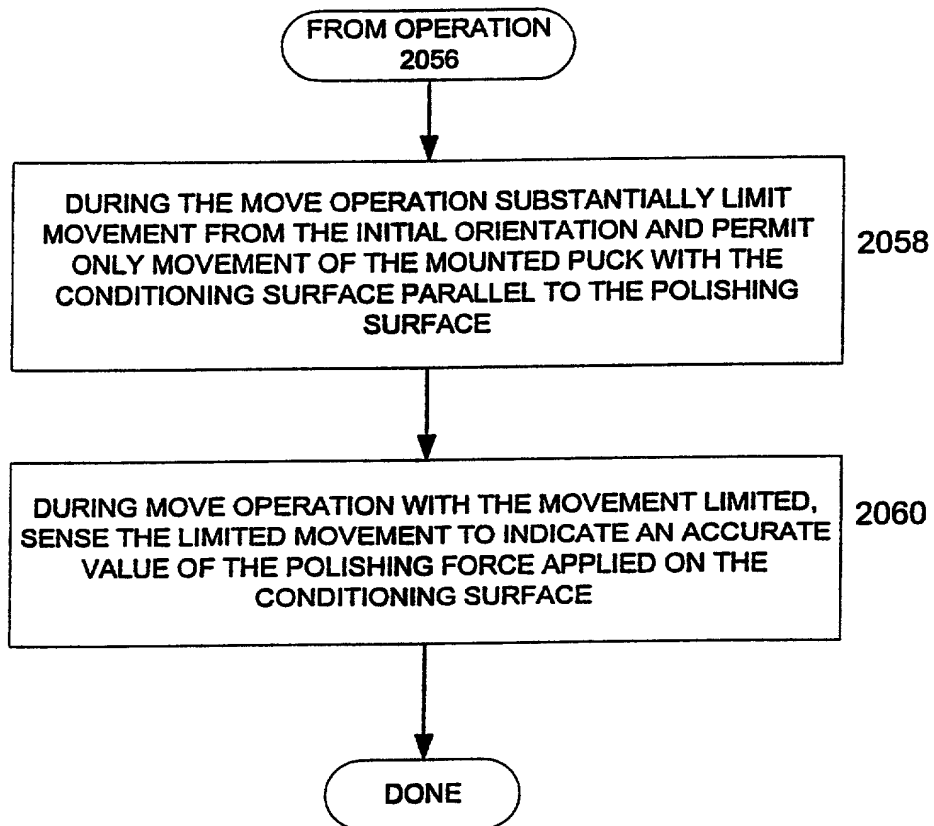


FIGURE 35

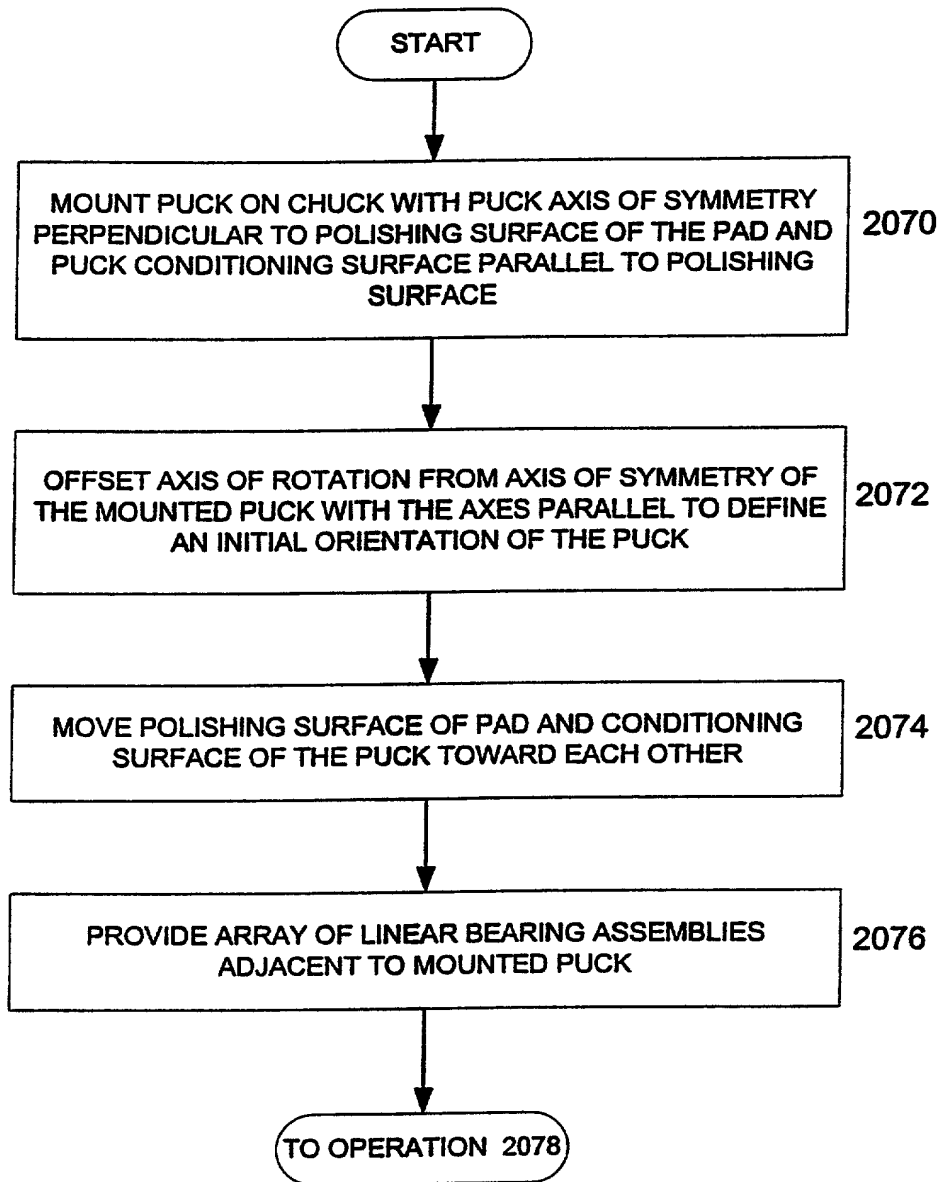


FIGURE 36

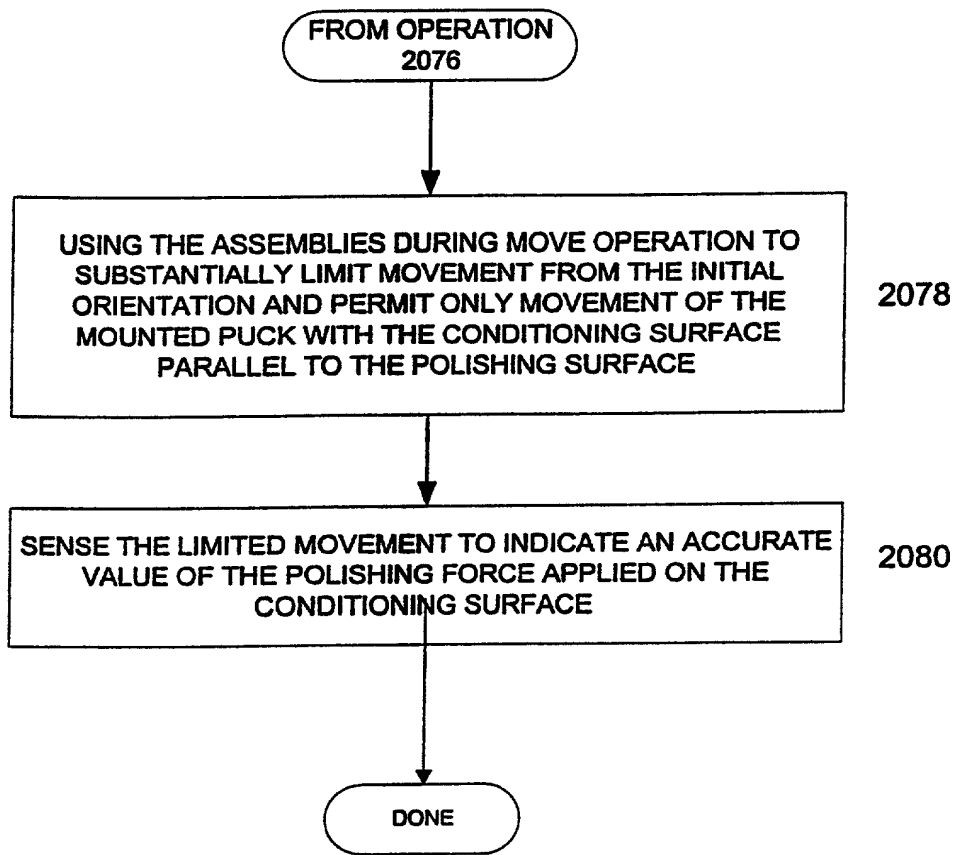


FIGURE 37

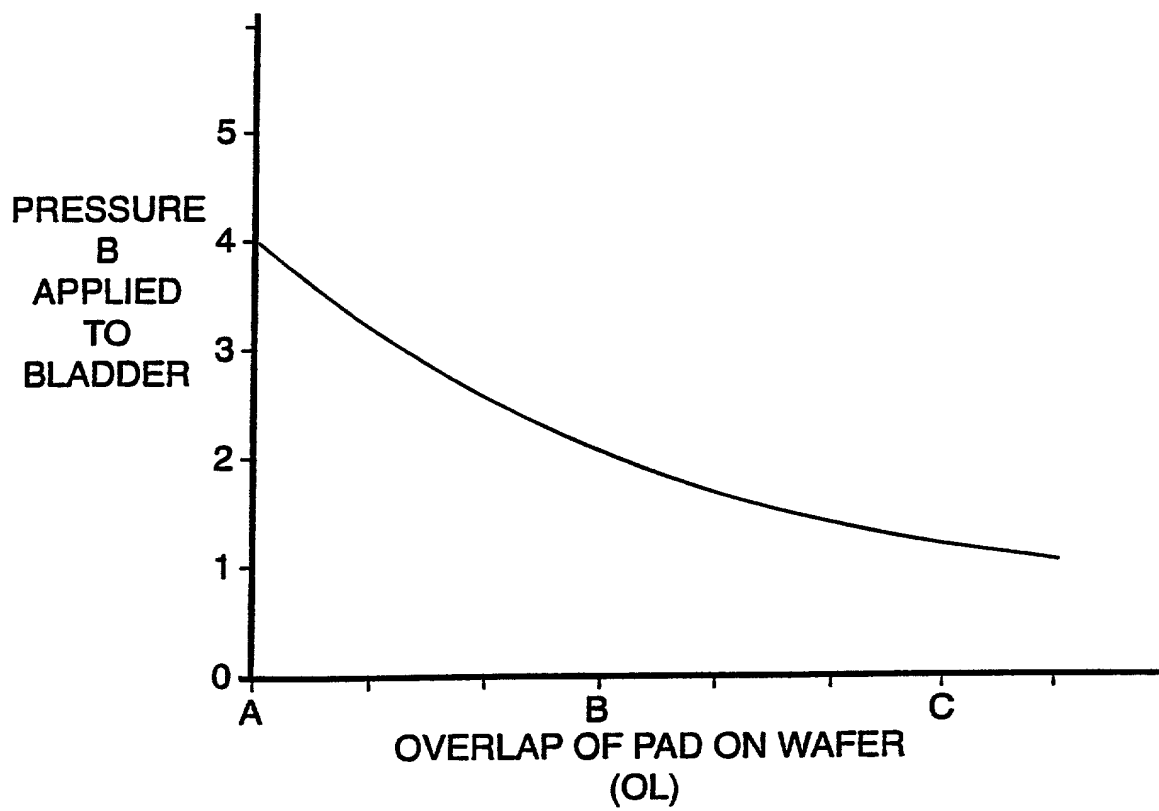


FIG. 38

5361

FIG. 40 is a block diagram of a system for controlling a wafer carrier, a puck head, and a retainer ring. The system includes a PC 2102, a MACHINE CONTROL O/S 2106, a METROLOGY 2160, a HARD DRIVE 2146, an ANALOG I/O 2179, a PAD MOTION 2360, an ENCODER 2156, a FORCE CONTROLLER 2300, and a FORCE 290. The PC 2102 is connected to the MACHINE CONTROL O/S 2106 via a bus 2104. The MACHINE CONTROL O/S 2106 is connected to the METROLOGY 2160 via a bus 2104. The METROLOGY 2160 is connected to the PAD MOTION 2360 via a bus 2104. The PAD MOTION 2360 is connected to the ENCODER 2156 via a bus 2104. The ENCODER 2156 is connected to the FORCE CONTROLLER 2300 via a bus 2104. The FORCE CONTROLLER 2300 is connected to the FORCE 290 via a bus 2104. The FORCE 290 is connected to the WAFER CARRIER 208, the PUCK HEAD 220, and the RETAINER RING 282 via a bus 2104.

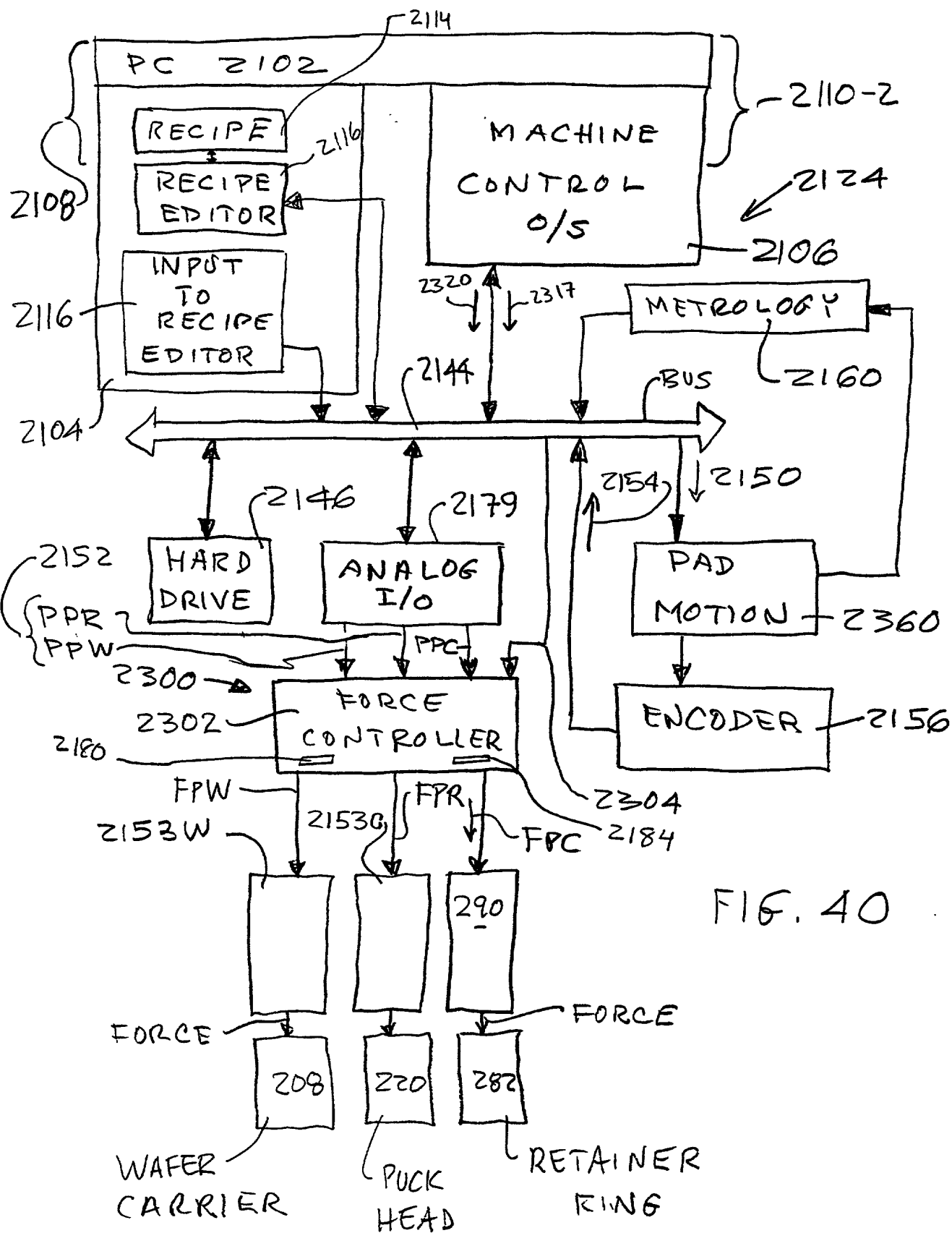


FIG. 40

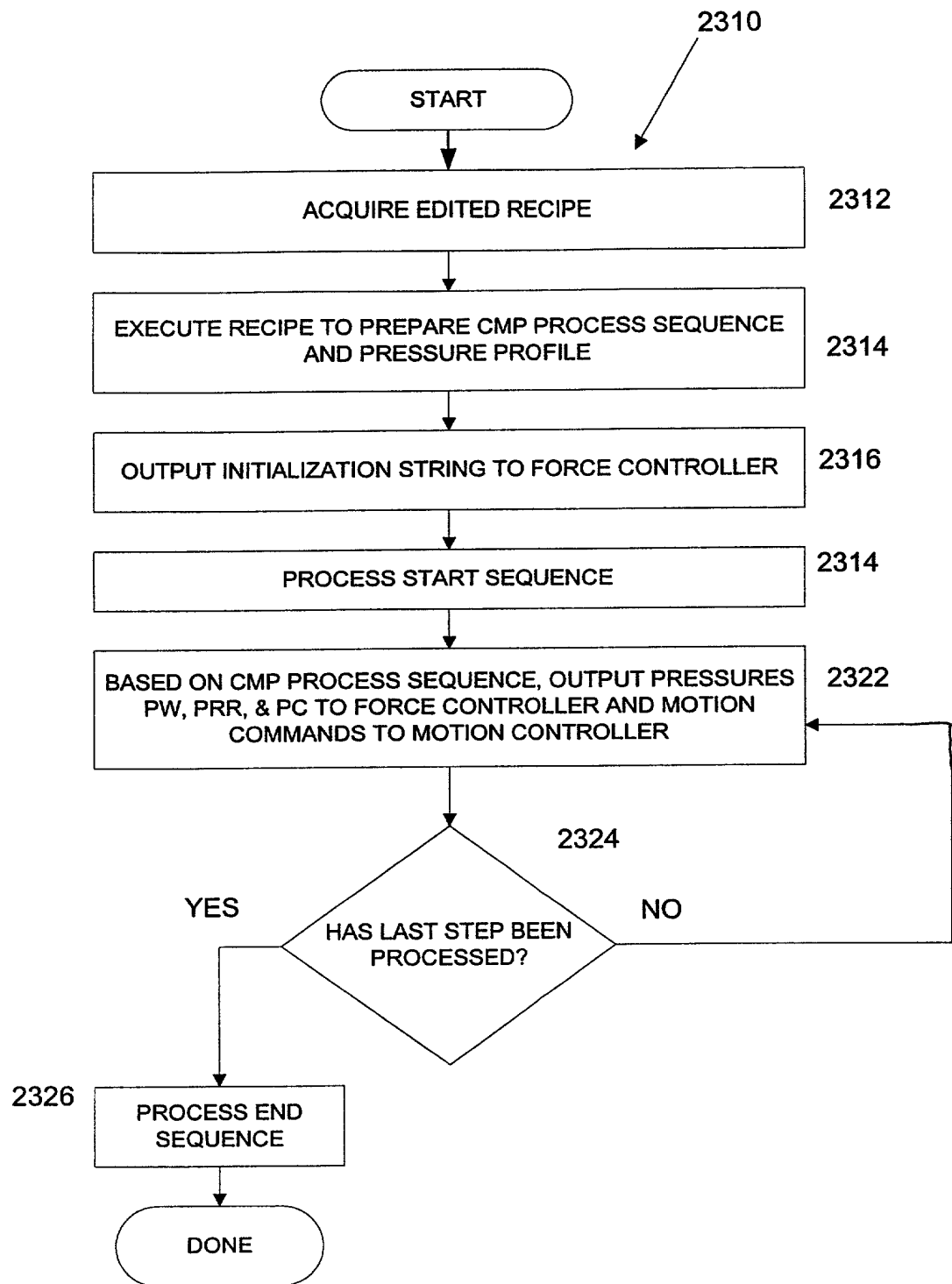


FIGURE 41

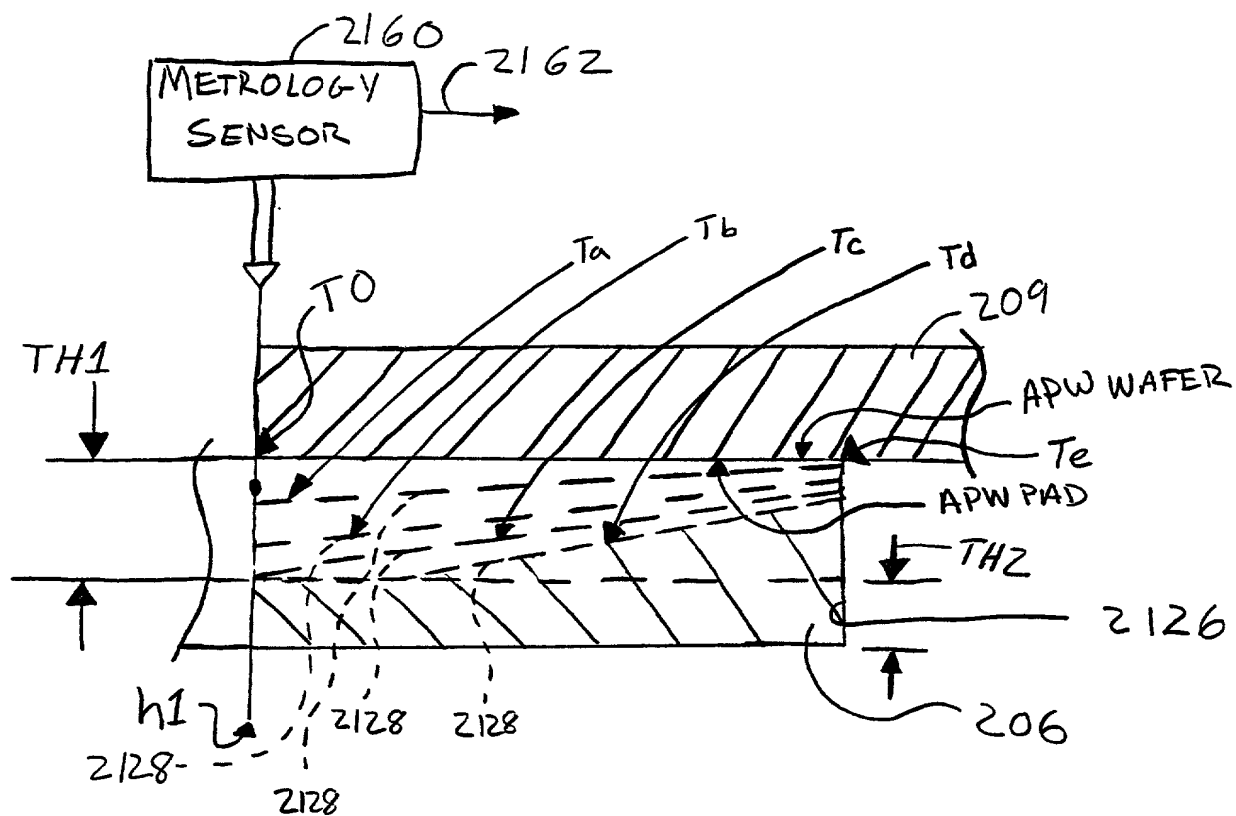


FIG. 42A

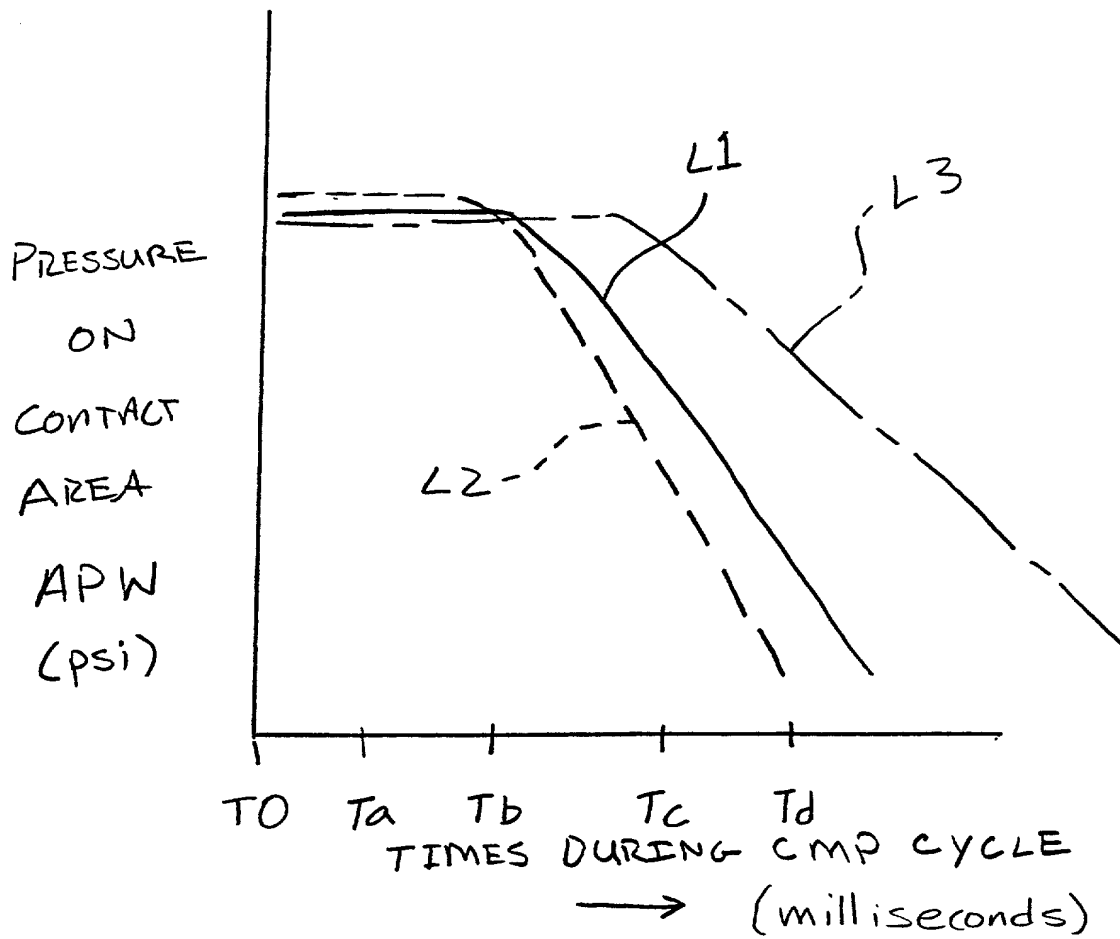


FIG. 42 B

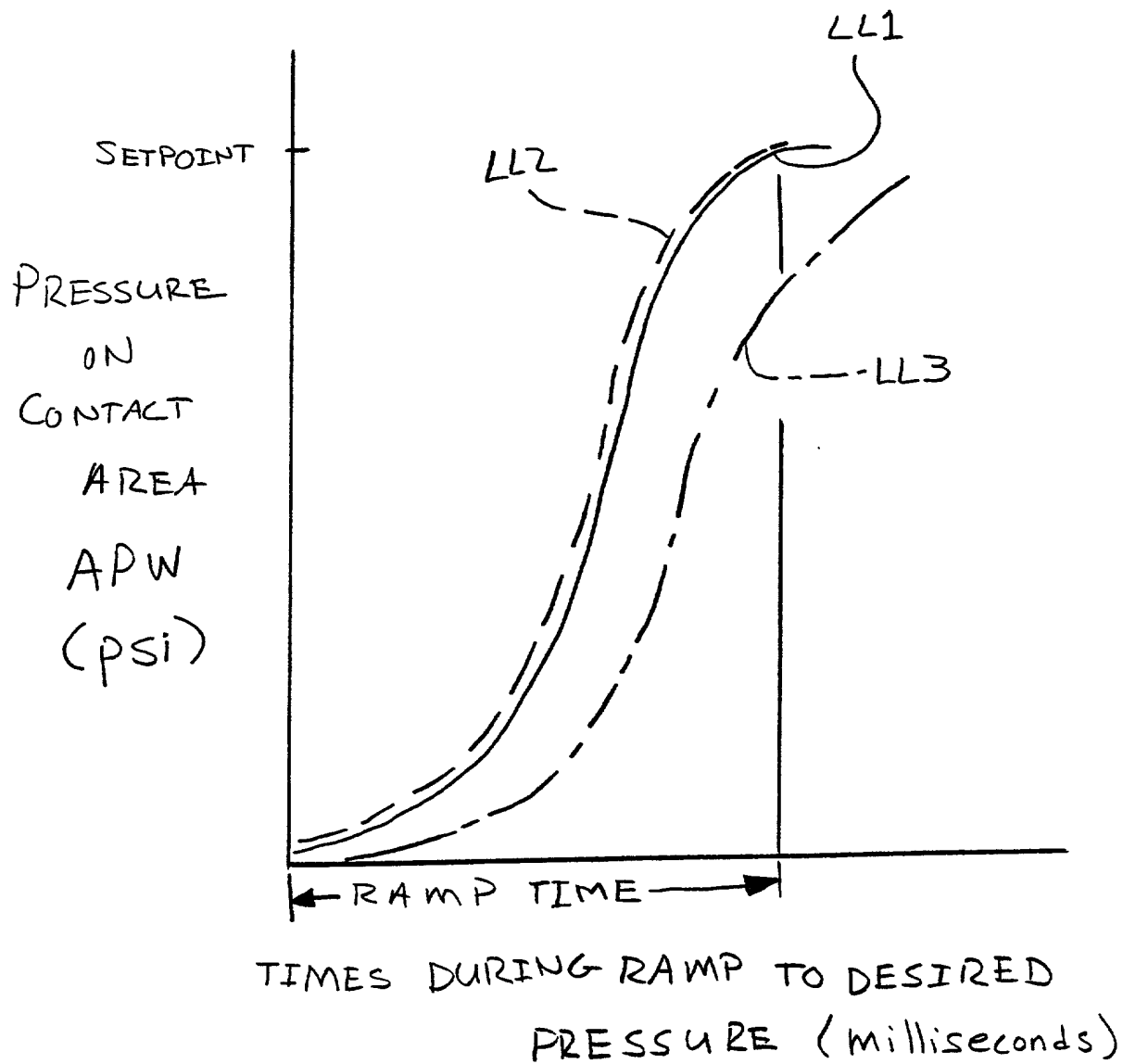


FIG. 42C

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99

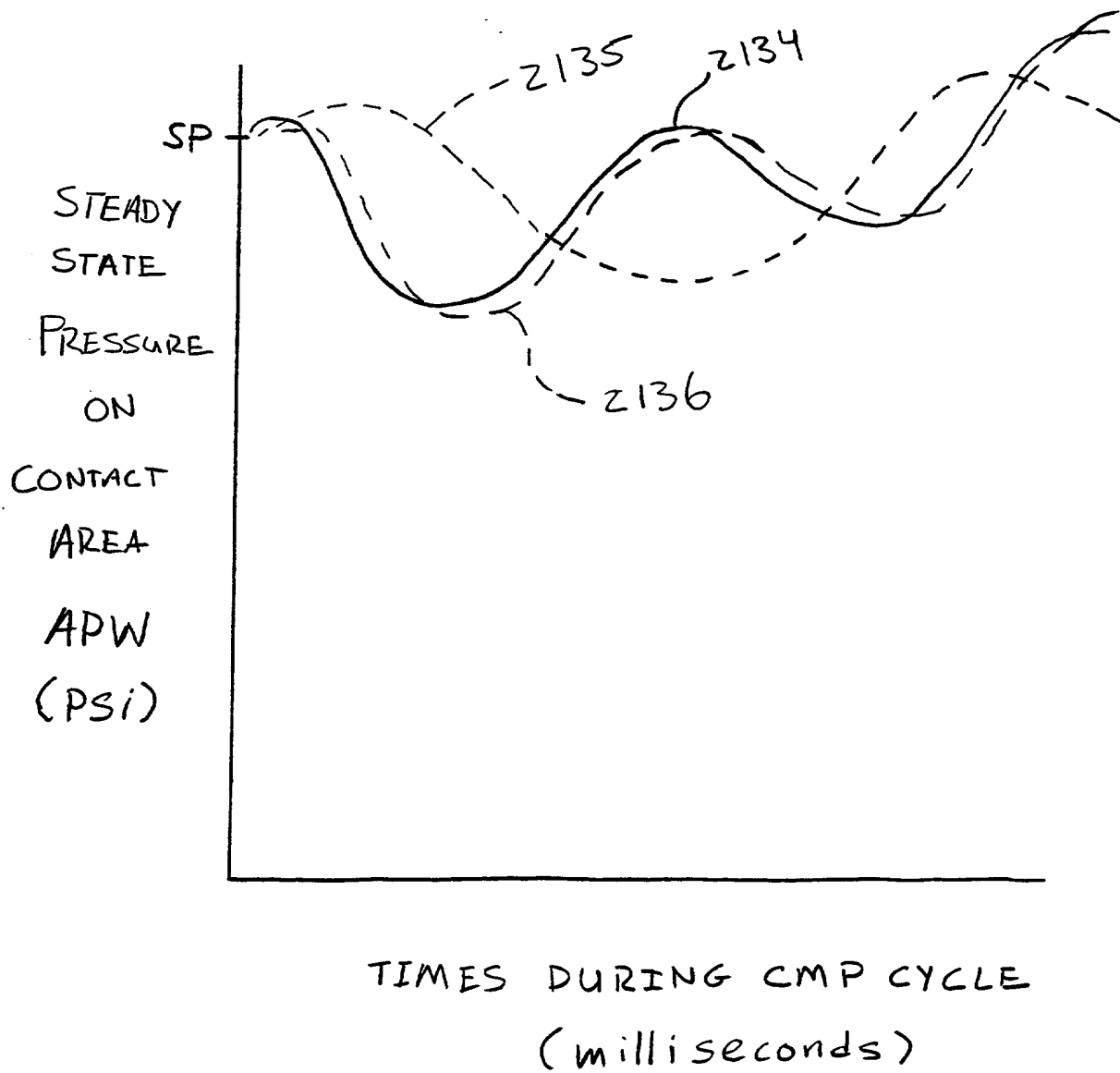
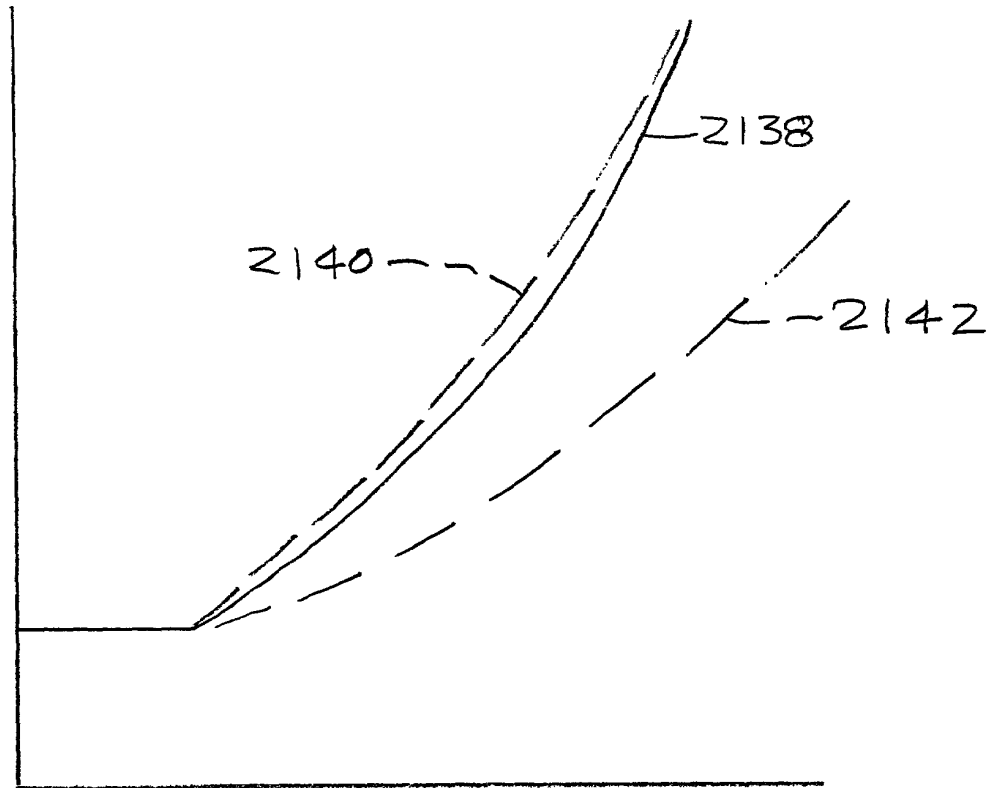


FIG. 42D

RELATIVE
POSITION
OF
WAFER
AND
PAD
(value
of
 h_3)



TIMES DURING STEP OF
CMP CYCLE
(milliseconds)

FIG. 42E

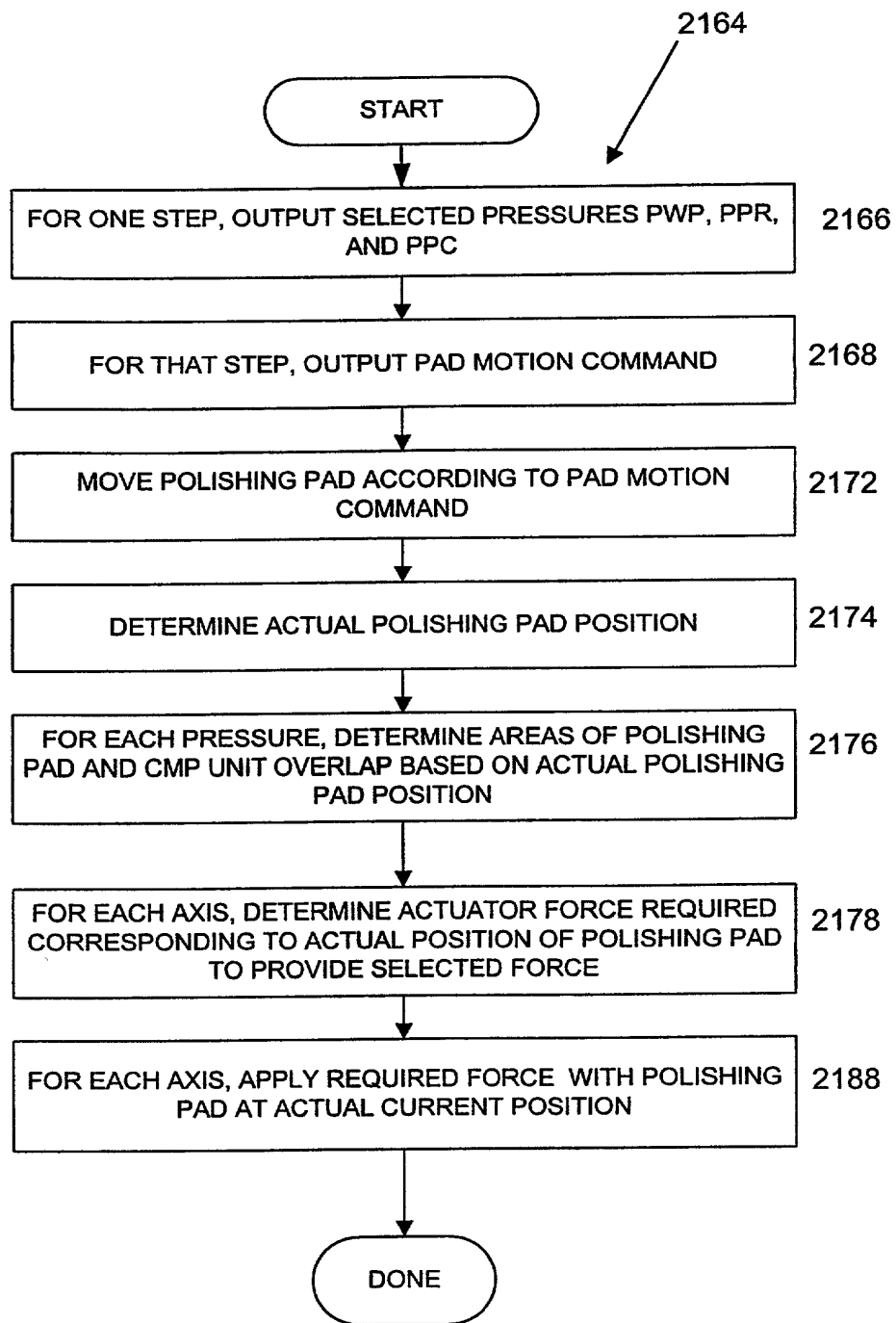


FIGURE 43

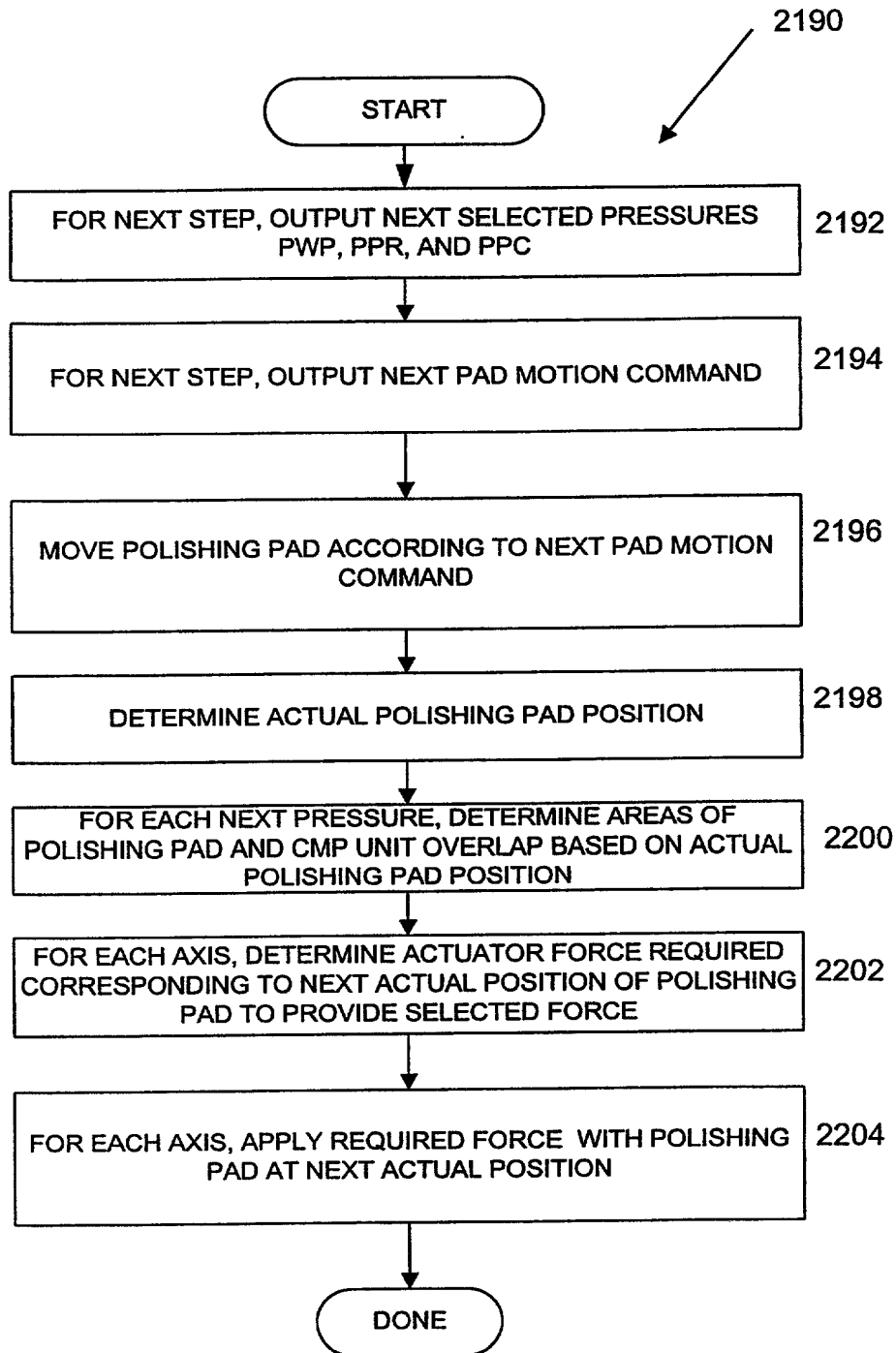


FIGURE 44

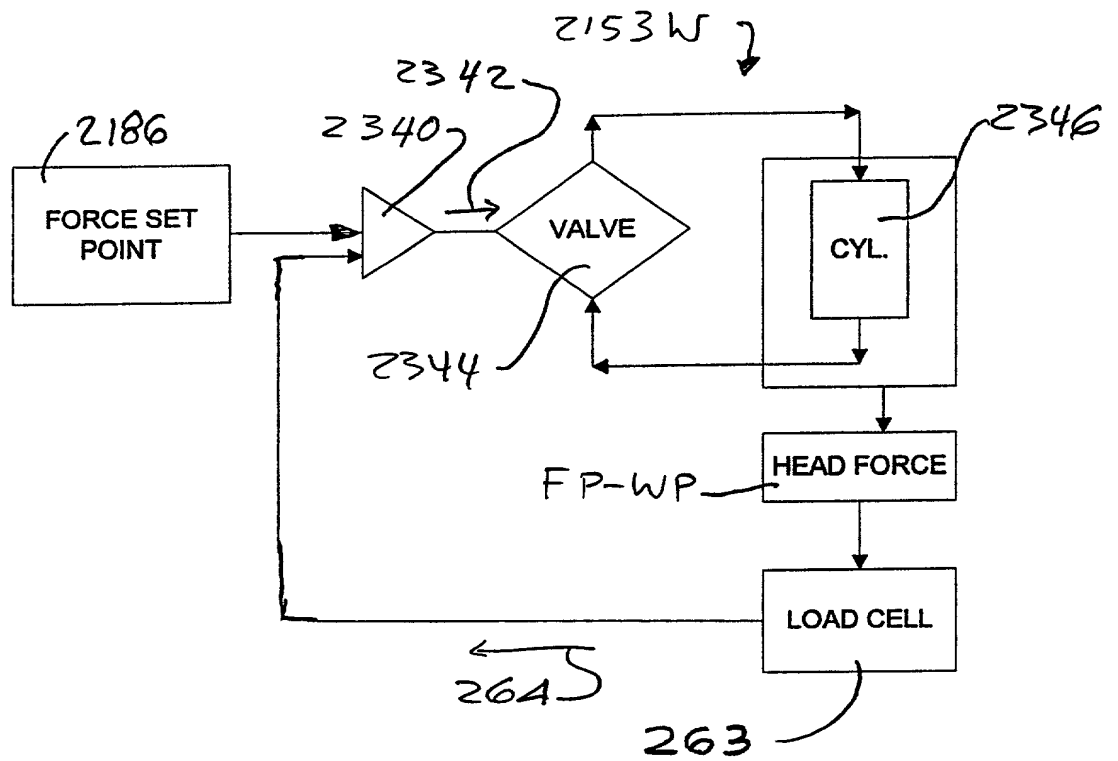


FIG. 45

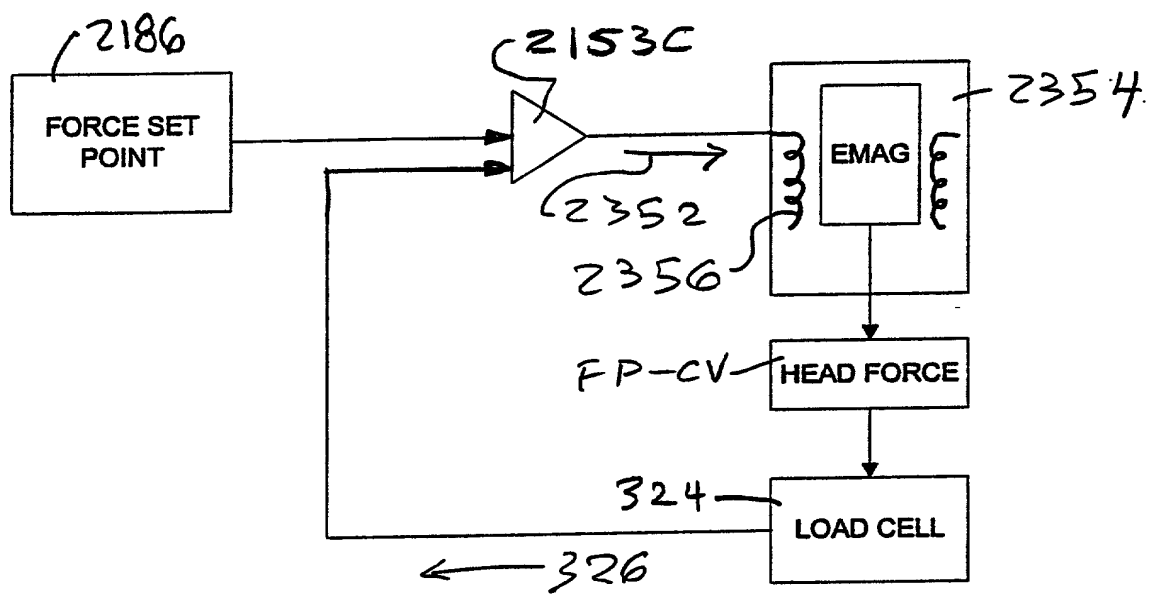


FIG. 46

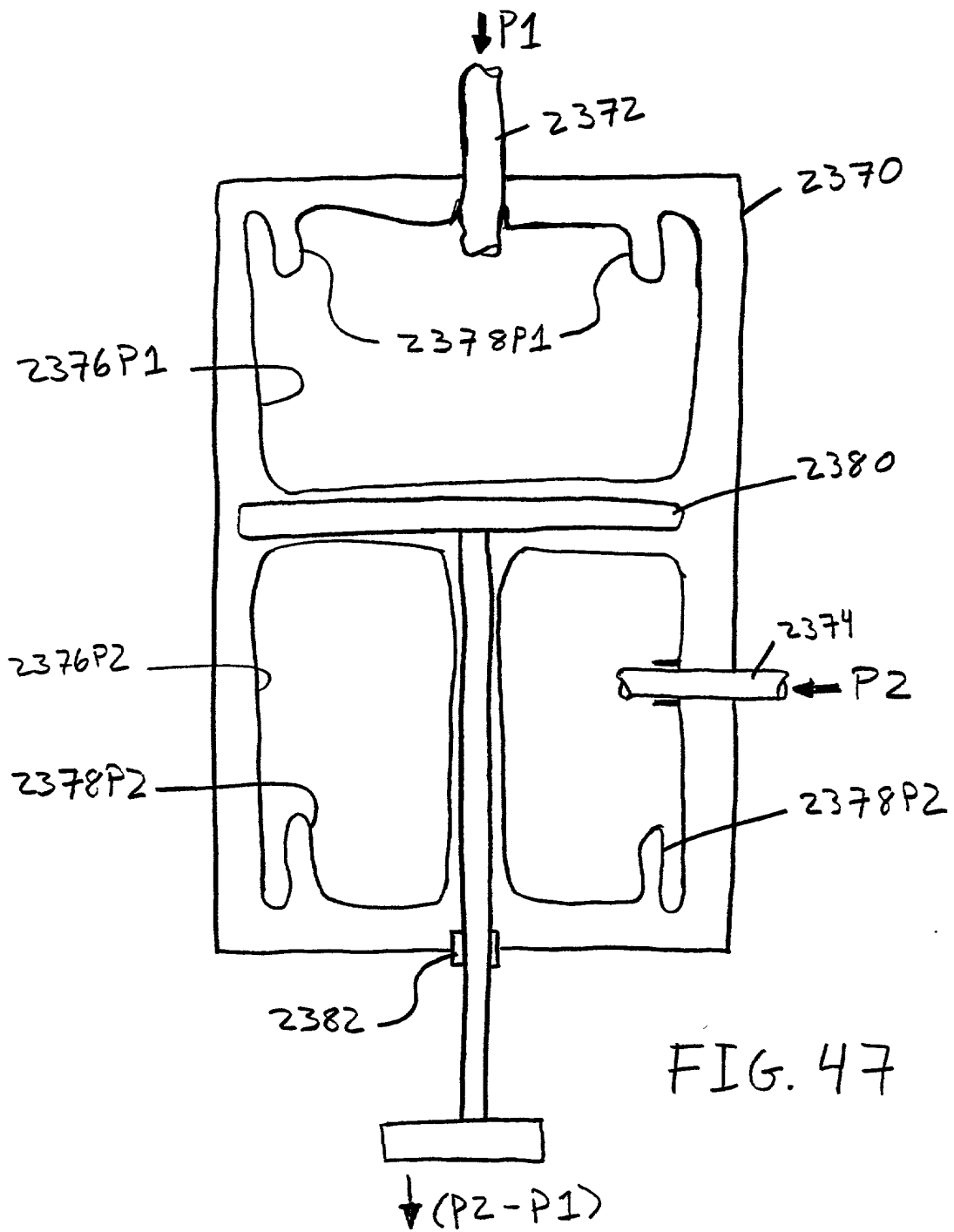


FIG. 47

